PRORISC/SAFE 2023

Poster Abstracts

10th - 11th July 2023

Chopping Techniques for a High speed (6GHz) CT DS ADC

Sundeep Javvaji, Muhammed Bolatkale, Kofi Makinwa, Lucien Breems

Advances in CMOS technologies have led to the development of continuous-time ΔΣ modulators (CTDSMs) with GHz sampling rates that achieve better than -100dBc linearity and bandwidths above 100MHz. However, at low frequencies (below ~10 MHz), their SNDR is limited by 1/f noise, which limits their use in radio receivers intended to cover both the AM and the FM bands. In this work, a multi-path multifrequency chopping scheme is proposed to suppress 1/f noise, while maintaining interferer robustness, noise, spurious, and linearity performance. Implemented in a CTDSM sampling at 6GHz, it reduces its 1/f noise corner frequency by 22x and achieves -98.3dBc THD, 122dBFS SFDR in 120MHz BW.

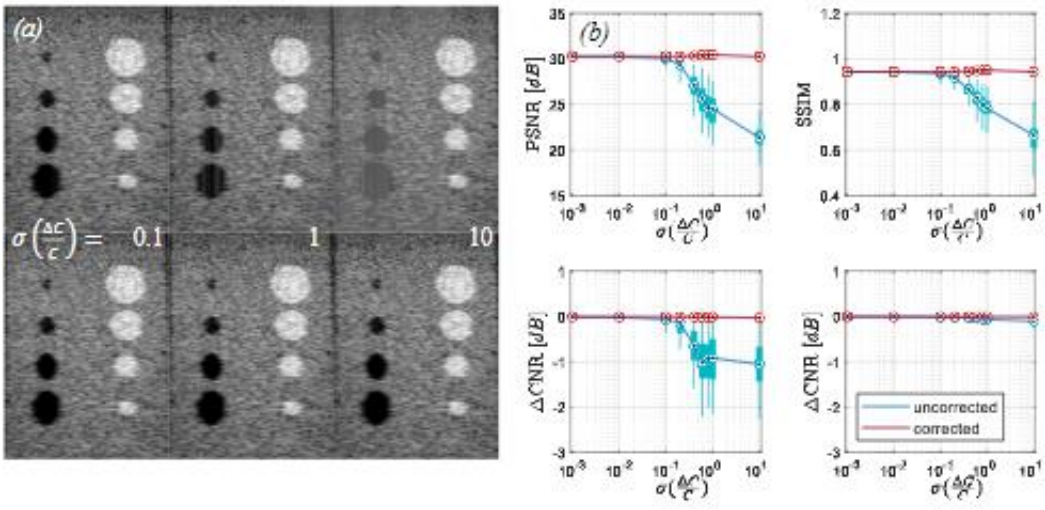
Effect of SAR-ADC Non-Idealities on Medical Ultrasound Imaging Modalities

N. Radeljic-Jakic, A. Flikweert, Y.M. Hopf, Z. Chen, N.N.M. Rosza, M.A.P. Pertijs

In traditional 2-D ultrasound probes, a 1-D transducer array is directly connected to an imaging system. With the introduction of 3-D probes that have 2-D arrays with thousands of elements, this approach has become impractical. Ultrasound ASICs can enable this transition by shifting part of the system functionality into the probe to reduce inter connect and cost. On-chip implementation of the analog-to-digital converter (ADC)has recently been shown to be particularly beneficial but comes with a significant power and area penalty. Current ultrasound converters are commonly implemented as successive approximation register (SAR) ADCs and designed following general-purpose design methodologies. In this work, the impact of SAR ADC non-idealities on postprocessed images is studied to achieve better trade-offs between performance and cost for ultrasound imaging.

This article provides a quantitative analysis of the impact of SAR ADC non-idealities on B-mode ultrasound imaging. In general-purpose SAR ADCs, effects such as capacitor mismatch, sampling noise, comparator noise, quantization error, clock skew and jitter introduce errors in the output of the ADC. However, due to the inherent averaging effect of beamforming, some of these errors have a limited effect on the image, enabling the use of architectures that would be unacceptable for the performance of general-purpose ADCs. RF-data captured from a Field-II simulation of a 128-element linear-array transducer with a 5 MHz center frequency is passed through a MATLAB model of a 12-bit SAR ADC where nonidealities are introduced.

Fig.(a) shows the effect of CDAC mismatch σ(ΔC/C) on the B-mode image of a cyst-phantom (40 x 55 mm) made before(top) and digital signal processing(bottom). After correction, even for the worst-case simulated mismatch of 10%, the effect on the image cannot be seen. This is confirmed by a 100-run Monte Carlo image quality analysis comprising 4 image quality metrics, as shown in Fig.(b), and implies highly relaxed CDAC matching requirements compared to conventional applications, allowing for a reduction of CDAC size and the associated power and chip area.



A Bias-Flip Rectifier with Duty-Cycle-Based MPPT for Piezoelectric Energy Harvesting

Xinling Yue, Sundeep Javvaji, Zhong Tang, Kofi A. A. Makinwa, Sijun Du

This poster proposes a DCB MPPT algorithm which finds the relation between the MPPT efficiency and the duty cycle of the bridge rectifier. The resulting equation shows that the MPPT efficiency only depends on the rectifier duty cycle, and it is independent of any other system variables, such as voltage bias-flipping efficiency, the open-circuit voltage from the harvester, vibration frequency, etc. It tracks the maximum power point by only regulating the duty cycle at a fixed value, simplifying the circuit implementation, and achieving automatic and continuous MPPT for piezoelectric energy harvesting.

A 13.56MHz Dual-Output Wireless Power Receiver with Voltage-Doubling Technology for Bioimplants

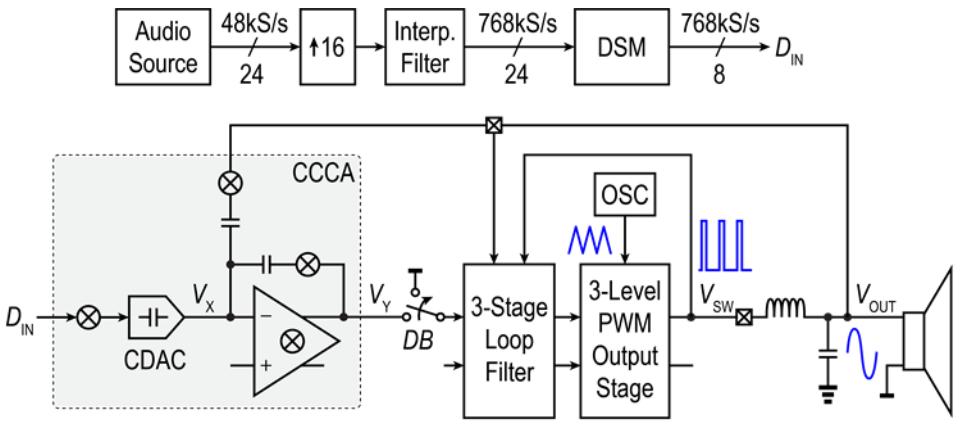
Tianqi Lu, Zu-yao Chang, Kofi A. A. Makinwa, Sijun Du

A regulating rectifier is highly desired in a wireless power transfer system for sub-100mW bioimplants. Such a rectifier simultaneously performs voltage rectification and regulation, thus avoiding post DC-DC stages. In this poster, a dual-output regulating rectifier with a voltage-doubling technology is presented. It achieves a better trade-off among PCE, VCR and power density, compared to state-of-the-art.

A 120.9-dB DR Digital-Input Capacitively Coupled Chopper Class-D Audio Amplifier

Huajun Zhang, Marco Berkhout, Kofi A. A. Makinwa, and Qinwen Fan

This paper presents a digital-input Class-D amplifier (CDA) achieving high dynamic range by employing a chopped capacitive feedback network and a capacitive DAC. Compared to conventional resistive-feedback CDAs driven by resistive or current-steering DACs, the proposed architecture eliminates the noise from the DAC and feedback resistors. Intermodulation between the chopping, PWM, and DAC sampling frequency is analyzed to avoid negative impacts on the dynamic range and linearity. Real-time dynamic element matching (RTDEM) is employed to address distortion due to mismatch in the DAC, while its intersymbol interference (ISI) is eliminated by dead-banding. The prototype, implemented in a 180 nm BCD process, achieves 120.9 dB of dynamic range and a peak THD+N of −111.2 dB. It can drive a maximum of 15W/26W into an 8/4-Ω load with a peak efficiency of 90%/86%.



Neuromorphic hardware for autonomous drones

Fabrizio Ottati, Jesse Hageenars, Luciano Lavagno, Guido De Croon, Charlotte Frenkel

Spiking Neural Networks (SNNs) are arising as a new computationally efficient paradigm in the field of machine learning. Despite this promise, the current market lacks a GPU-equivalent for neuromorphic computing, leaving a gap in the availability of specialized hardware tailored to the unique requirements of SNNs. A hardware platform that can satisfy these needs is the Field Programmable Gate Array (FPGA). However, deploying an SNN model to FPGA requires hardware design know-how, which leads to full-custom implementation that can hardly be expanded or repurposed. Here, a high-level synthesis approach to this problem, hls4nm, is proposed, testing it on the use case of lower power, autonomous tiny drones. A convolutional SNN (CSNN) is trained on event-based camera data and outputs low-level control actions for performing autonomous vision-based flight. The neuromorphic pipeline is currently deployed to Intel's Loihi prototype neuromorphic processor, that runs 4 neural networks in parallel on the four corners of the image, sharing the same model, that estimate optical-flow to allow autonomous operation of the drone. Due to the Loihi system large power footprint (approximately 5W), it requires a large battery and, thus, it is deployed to a large droneweighing 1 kg.We are targeting a smaller drone, the CrazyFlie 2.1, weighting 27 g, with a power budget for the payload of 300mW for the whole payload (control, neuromorphic hardware and event-based camera). Thanks to a hardware-algorithm codesign, we have minimized the memory footprint of the model to around 800 Kib, which allows targeting a small AMD Xilinx FPGA to minimize chip area and power consumption. This is coupled with a Prophesee eventbased camera sensor. The SNN model is translated to a C++ description, ported to hardware using high level synthesis (Vitis HLS [7] and Vivado). This allows for fast deployment and design space exploration, thereby addressing the lack of flexibility of full-custom approaches. A fully parallel architecture is used to keep latency under 5 ms while drastically reducing clock frequency to minimize power consumption. The four corners are processed all in parallel in the hardware via line buffer data structures. Since Look-Up Tables (LUTs) are the most power-hungry components on an FPGA, the network is mapped to Digital Signal Processor (DSP) macros available on AMD Xilinx FPGAs. To allow for maximum parallelization while keeping a low resource usage, which is compatible with small-scale FPGA devices, DSP fine-tuning and programming is used to perform a Single Instruction Multiple Data (SIMD) dataflow. In this way, the network runs on approximately 120mW, with a clock frequency of 25 MHz, using around 50 DSPs.

PIN-Detector ROIC for Single-Electron Detection with High Time-Resolution

Alireza Mohammad Zaki, Stoyan Nihtianov

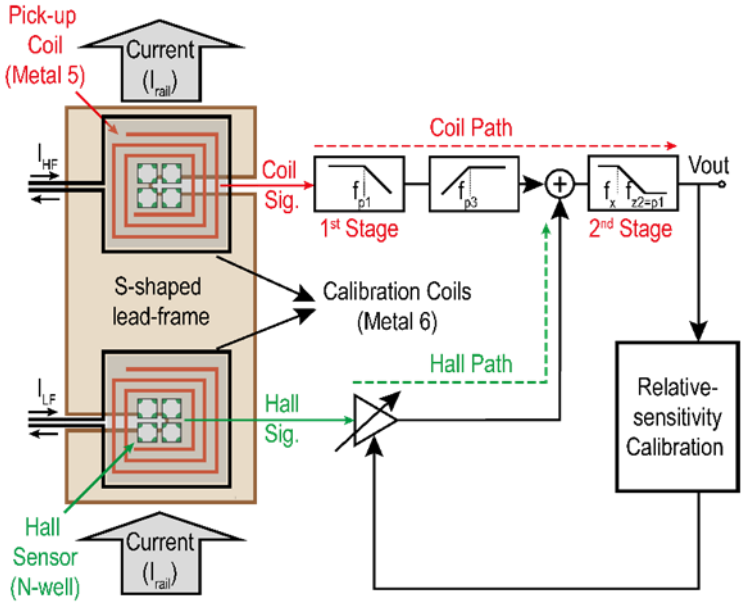
Single-electron detection is used for a wide range of applications: advanced industrial process control, experimental physics and space instruments, and material testing and medical imaging. These applications give rise to the development of a wide variety of charge-sensitive readout integrated circuits (ROICs). State-of-the-art imaging systems, such as scanning electron microscopes (SEMs), demand the ability to detect small amounts of charge with high time-resolution and limited power consumption. These requirements are interpreted as designing low-noise and low-power readout electronics with a low detection error rate and small silicon area occupation, allowing the pixelization of the detector area. This poster presents the methodology and experimental qualification results of a state-of-the-art, high time-resolution, low-noise, and power-efficient charge-sensitive ROIC intended for counting single-electrons detected by a silicon PIN detector. The ROIC is designed in TSMC 40-nm MS/RF CMOS technology to detect charge portions as small as 160 aC, delivered randomly by the detector at a maximum of 4×108 hits/s, with 0.33 mW/pixel power consumption. For every charge pulse of the detector, the ROIC generates voltage signals with a peak amplitude of 25.9 mV, a rise time of 2.4 ns, and an SNR above 18.

A Self-calibrated Hybrid Magnetic Current Sensor with a Gain Drift Temperature Compensation Scheme

A. Jouyaeian, Q. Fan, M. Motz, U. Ausserlechner, K. A.A. Makinwa

Magnetic current sensors are widely used in applications where both galvanic isolation and wide bandwidth (BW) are desired, such as switched-mode power supplies and motor drivers. Hall-effect current sensors are a common choice in standard CMOS designs. However, their resistance results in a fundamental trade-off between BW and resolution, which limits their use in high-frequency applications. On the other hand, coils have a differentiating characteristic. Thus, they can achieve much wider BW and resolution, but it has the drawback of not sensing DC currents. Wide-band hybrid sensors can then be realized by using Hall-effect current sensors for low-frequency signals combined with coils for the high-frequency ones.

This work presents a hybrid current sensor that measures the differential magnetic field around a lead-frame S-shaped current rail. The induced magnetic field is sensed by two differentially connected on-chip coils built on top of quad-Hall sensor structures. By sensing the coil current and employing a pole-zero cancellation scheme, its front-end achieves high DR and resolution without external components. Compared to state-of-the-art, it achieves similar BW (5MHz), but with 7.5x better resolution (43mArms) and 50% less chip area (3.9mm2).



Reliable low latency wireless intra aircraft communication

E.S. Bertram

Conventional data networks inside airplanes have traditionally been fully wired, however these wired networks come with the drawback of increased maintenance complexity and weight. To overcome these issues, wireless solutions can be used, given that they support the latency and reliability requirements of the network. To this end, software defined radio solutions that exploit diversity in the channel can be used. An implementation of this, based on discrete time FIR filters is proposed, which separates the complex mixing of all signals in the shared channel, into orthogonal streams. This can in turn be used for nodes in the network to access individual sources in the channel, without being interfered by other sources in the channel. To verify its usefulness inside aircraft, channel measurements have been performed and a test chip has been designed, the preliminary results of which will be presented.

Multi-purpose Millimeter-wave Circuits for Both Wireless Communications and Radar Sensing

Y. Hou, V. Vidojkovic, D. Milosevic

Future generations of wireless communications (6G) and radar-sensing will heavily rely on the use of millimeter-wave frequencies in the range between 24-150 GHz. As a result, many communications and sensing nodes operating in different frequency bands will be introduced. Each of those systems will use the concept of active array antennas to allow electronic beam steering to compensate for the high path loss at these high frequencies. A new and innovative highly integrated shared-aperture active antenna concept is introduced to accommodate emerging millimeter-wave sensing and communication applications. It aims to provide multi-band and multi-mode operation using a single active array aperture, significantly reducing the overall system cost and space requirements. The intended use case includes but is not limited to switching frequencies for either high resolution or long-range radar application, or using radar function to perceive the environment and switch to proper frequency band for wireless communication.

This work focuses on the development of critical building blocks (mixers and power amplifiers) for multi-band multi-mode RFICs which support shared-aperture arrays. Main challenges include multi-band circuit design, PA that can support radar application while still meet strict EVM requirements. Possible solutions would be to implement high tunability, explore compact multiband matching networks and/or experiment PA structures which are not commonly used at millimeter frequencies.

Mi-RAYS: Power-efficient 140GHz Transmitter Architectures for Next-Generation Automotive Radar

R. Schalk, M. Neofytou, G. Radulov, V. Vidojkovic, K. Doris

Automobiles for mass deployment were introduced in the early 1900s as purely mechanical systems. Over the last decades, automobiles have evolved to electromechanical devices where the innovations are driven by electronics. Nowadays, vehicles are comprised of more than 100 sensors in over 30 systems including performance monitoring of mechanical systems and integration of Advanced Driver Assistance Systems (ADAS). Mature and cheap integrated circuits for mmWave radar sensors are the foundation of these ADAS systems. The target for new generation of ADAS systems is to enable fully autonomous driving systems that will allow for significant reduction of human life loss from traffic accidents, improve traffic flow and reduce CO2 emissions. These substantial societal benefits are enabled by level 5 drive automation, which requires much higher resolution and robustness of mmWave automotive radar. Cognitive perception by means of Artificial Intelligence requires increased resolution in distance, velocity and angle of arrival to enable small object classification (e.g. debris on the road) and eventually enable detailed mapping of the environment. This is not possible with current-day automotive radar systems. Additionally, it is envisioned that more than 10 radar sensors will be embedded into future generation cars. The drastic increase of sensors in the field will inevitably introduce concerns for vehicle-to-vehicle interference, which needs to be addressed. Using the 140GHz band for next-generation radar transceivers can achieve such requirements. The smaller wavelength and larger available bandwidth can advance radar resolution and reduce sensor size, similar to the transition from the 24GHz to 79GHz band. However, this transition comes with significant challenges that must be overcome. These include increased path losses, silicon technology limitations in signal power and noise, and significant losses originating from the mmWave IC and antenna interface. Very large-scale MIMO and/or phased array schemes with multiple transceiver chips and antennas will be required to overcome these challenges, and are to be combined with waveguide launchers with in-package antennas. For interference mitigation, transceivers need to support the synthesis of advanced waveforms enriched with digital coding schemes, interference detection schemes, multiple polarizations and adaptive beam patterns, and even transmit receive coordination based on standardized channel access schemes. These imposed requirements of high power, high efficiency and high flexibility find potential solutions in a direct digital-to-RF transmitter topology. Digital transmitters can offer increased efficiency compared to classical analog transmitter chains intended for variable envelope signaling, since these are often employed in power back-off to reduce signal compression and realizing sufficient signal integrity. Radar is commonly based on constant envelope signaling, whereas this direct benefit of digital transmitters does not hold. Nevertheless, digital transmitters can form the basis for next-generation mmWave radar transmitters, since they allow for operation in maximum Power Added Efficiency (PAE) window, while allowing for constant envelope signaling and variable envelope digital coding schemes. Targeting efficient LO distribution, low-loss passives, confinement on waveform support and transmitter topology is required for optimal system design.

A 3-320 fJ/conv.step Continuous Time Level Crossing ADC with Dynamic Self-Biasing Comparators Achieving 61.4 dB-SNDR

M.W. Timmermans, K. Oosterhout, E. Cantatore

This paper presents a level crossing ADC (LC-ADC) for biomedical applications. The ADC uses dynamically biased comparators, which require minimal power when the input voltage is far away from a decision threshold. This results in >10x better power efficiency compared to prior LC-ADCs when converting sparse signals. In a 16 kHz bandwidth, the LC-ADC achieves a 61.4 dB SNDR resulting in an efficiency of 3 fJ/conv.step for sparse input signals.

Transistor Based Source Degeneration: A Comparison Between Active and Resistive Degeneration

Kyle van Oosterhout, Martijn Timmermans, Marco Fattori, Eugenio Cantatore

This paper introduces a source degeneration technique using a diode connected transistor as degeneration device rather than a conventional resistor improves the robustness against changes in biasing condition and temperature, and removes the need for calibration. The method is validated using an analytical model, as well as with simulations, both at very low bias currents (where the analytic exponential model matches the behaviour of the transistor very well) as well as closer to the threshold. The method shows an improvement of 6dB to 20dB in linearity when variation of bias current and temperature of 20% are considered. Using this technique would thus enable highly linear, power efficient, open-loop amplifiers without the need for calibration systems, which have an unavoidable power and area overhead.

A Scalable and Flexible Haptic Skin for Robotic Applications

Jixuan Mou, Marco Fattori, Eugenio Cantatore

In recent years, robotics and its exploitation in commercial applications have experienced a significant revolution. The strong increase of robots employed in industrial automation has promoted the demand for robots capable to execute more complex and less intuitive tasks, even in unstructured environments and in presence of humans. One of the drivers of this revolution in robotics is related to the advent of artificial intelligence (AI). The application of camera-based vision systems and voice recognition systems have been successfully demonstrated to enable 3D-pose object estimation in partially structured environments. In order to explore the potential of versatile interactions between robots and humans (in unstructured environments), additional sensing information, such as touch, temperature, proximity and proprioception, are necessary to reduce the uncertainties in the interaction modalities, by complementing vision and hearing sensory data.

In this project, a scalable, flexible, and stretchable sensor array will be designed and prototyped. The sensors are distributed on a flexible substrate, where customized silicon chiplets are placed close to sensors for readout, data management and dispatch purposes. A relatively high sampling rate (~ksample/s) per sensor is required by the applications, hence conventional synchronous sampling and analog-to-digital conversion techniques would lead to a tremendous throughput of data to be sent, processed and stored. The data communication needs could easily reach the bandwidth limit of existing protocols, such as I2C, CAN-BUS, etc... Moreover, the latency introduced by the processing of such a large amount of data could have a detrimental impact on the robot manipulation.

This work is mainly focusing on the design of a network utilizing custom silicon chips, where in each node (single silicon chip) touch (pressure) sensors will be digitalized. As touch events are generally sparse, level crossing ADCs can be deployed to efficiently perform the analog to digital conversion while dramatically reducing the data rate and the energy required for data dispatch.

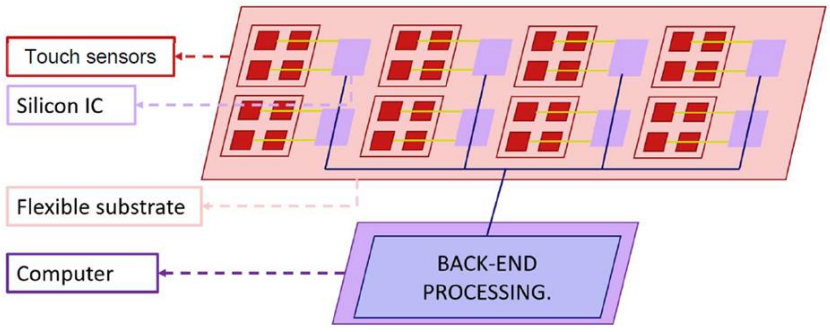


Figure 1. A conceptual system architecture.

Post Calibration of Sigma Delta Analog to Digital Converters Based on Machine Learning

Leonardo Papale, Marco Fattori, Eugenio Cantatore, Lucien Breems

The systematic downscaling of CMOS Integrated Circuit (IC) technologies has enabled unprecedented improvements in transistor density, frequency of operation, energy efficiency, and reliability. While technology downscaling has been extremely beneficial for digital circuits, the design of analog frontend electronics and Analog-to-Digital converters (ADCs) in deep sub-micron CMOS technologies is becoming increasingly challenging due to the systematic power supply reduction, the intrinsically larger device parameter variability, and the higher low-frequency noise level of these transistors. Moreover, to ensure the system target performance with a relatively large sigma coverage as required e.g. by the automotive market, accurate calibration loops are needed to precisely compensate circuit non-idealities. The calibration of static and dynamic first-order errors has been widely investigated. However, calibrating circuits with predictive models to account for multiple higher-order errors over time, process, supply voltage, and temperature (PVT) variations is still a grand challenge. In this scenario, the capabilities of Machine Learning (ML) models to learn complex input-output relationships is a promising alternative to implement novel calibration algorithms. Moreover, ML solutions are in principle able to adapt to device-specific nonidealities and compensate for them, leading to a potential enhancement of the overall system performance reliability. In the existing literature, several ML-based calibration solutions have been already reported to compensate for the nonlinearities of specific architectures, such as time-interleaved or pipelined ADCs, leading to relevant improvements in the Equivalent Number of Bits (ENOB). Our work focuses on the use of ML-based calibration solutions to compensate a wide range of nonidealities even over PVT in Sigma Delta ADCs. This compensation scheme uses a feedforward approach based on a pre-trained neural network to which several relevant features extracted from the system are fed. The neural network is thus used to predict the converter nonidealities and its output to calibrate the converter bitstream. Since the calibration is performed in the digital domain, this approach is expected to benefit from the transistor downscaling and thus, the hardware implementation of these ML calibration circuits has the potential to require a negligible area and power, when compared to the ADC, while introducing a relevant enhancement of the overall system performance.

A single molecule detection system comprising large area, low-cost organic addressing electronics and a Si high dynamic range front-end

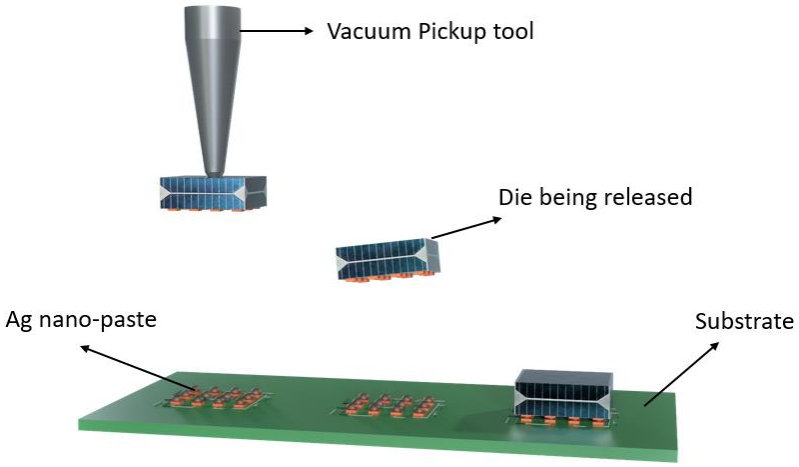
Enrico Genco, Eugenio Cantatore

Single-molecule level analysis is the future frontier in precision healthcare. Bioelectronic systems recently attracted great interest due to their exceptional sensitivity for protein biomarkers detection in physiological environments. In this work, a 96 biosensing elements prototype with enhanced sensing capabilities and made of novel materials is discussed. The biochemistry assay system is based on a matrix of Electrolyte-Gated Organic Field Effect Transistor (EGOFET) sensors, flexible addressing logic and a high-accuracy Si Application-specific integrated circuit (ASIC) providing front-end and data conversion functions. Time Domain Multiplexing (TDM) is used to reduce the number of lines needed to read the sensors output currents. A current sensitive front-end with a dynamic range of more than 120dB is achieved with a 12bit oversampled ADC and a programmable gain transimpedance amplifier, enabling the detection of proteins down to the single molecule concentration level. The proposed solution leads to a low-cost and extreme sensitivity system, successfully integrating devices made with three different technologies and materials. These results pave the way for the development of complex systems based on a matrix of bio-electronic sensors and a miniaturized Si IC chip for data processing.

Novel pressure-less bonding through silver nano-paste for contactless die-to-substrate attach

Ahmed Abdelwahab, Henk van Zeijl, Massimo Mastrangeli

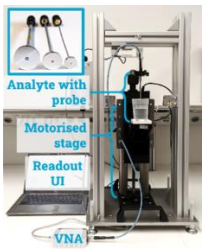
We present novel insight into pressure-less bonding and sintering for contactless die-to-substrate attach for advanced packaging. Bonding and sintering of millimeter-sized dies were achieved using commercially available silver nano-paste (DM-SSA-10300S, Dycotec Materials), with no pressure applied during both the chip placement and the sintering steps. Die bonding was implemented using a semi-automatic die bonder (T-3000-PRO, Tresky), with dies picked, aligned and released through a tailored contactless process. The dies were optically aligned in proximity to the substrate and released from the vacuum gripper without any physical contact with the substrate. To evaluate the compatibility of the paste with different surface metallurgies, the surface of the dies was patterned silver (Ag), gold (Au), copper (Cu), and aluminum (Al), respectively. Additionally, the surface of the substrates was correspondingly prepared with Ag, Al, Au, and Cu, to compose a matrix of different layer combinations. A stencil mask with a thickness of 50 □m was used for depositing the paste on the substrates, resulting in 50 □m bond line thickness. After the tailored Pick-and-Release process, the nano-paste was thermally cured through a two-step process: initial drying at 80 °C for 10 minutes, followed by sintering at 250 oC for 30 minutes, both performed in air. After bonding, the bond strength was evaluated through mechanical shear testing. Preliminary results indicate that the Pick-and-Release bonding approach using commercially available silver nano-paste enables successful contactless die attach, and shows compatibility with different metallurgy combinations. The shear test results demonstrate satisfactory bond strength (in the order of several MPa), suggesting the potential for this technique to be employed in advanced packaging applications.

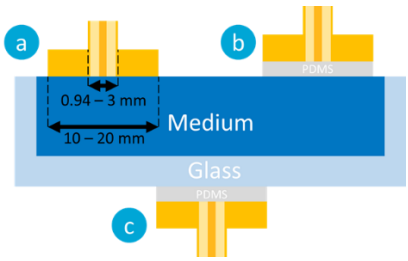


Dielectric spectroscopy for non-invasive sensing of multi-layered organ-on-chip devices

Timothy B. Hosman, Massimo Mastrangeli and Marco Spirito

The rising costs and duration of pharmaceutical research and development (R&D) negatively impact the time-to-market for new, affordable and effective drugs. Over the last decade, organ-on-chip (OoC) technology has emerged to address this issue, aiming to develop accurate in-vitro models of human organs. OoC models could be applied in pre-clinical drug testing, aid in personalised medicine, and leverage the ethical burden of animal-based drug studies. To advance time-continuous non-invasive monitoring – a main unmet need in OoC applications – we propose dielectric spectroscopy (DS) as a sensing technology. The dielectric spectrum depicts a material's response to an electric field across frequency, which is unique for any given material [3]. Therefore, DS could hypothetically identify specific cell contents and concentrations in media, and extract cell properties such as cell size, permeability and cell membrane thickness. Furthermore, DS is label-free and non-invasive, making it in principle ideal for sensing applications in OoC. Identifying layer-specific spectral information from the cumulative dielectric response of stacked multi-material layers, as occurring in OoC devices, is central to this endeavor and hereby addressed. In the running implementation, DS is conducted using a vector network analyzer (VNA) connected to a flanged open-ended coaxial line (Fig. 1), calibrated to the medium surface using three different reference liquids. The probe can be vertically positioned with micron accuracy using a motorized stage and a load cell (Fig. 1). Using a lookup table-based numerical model, the measured field reflected from the tested medium is converted to a dielectric spectrum [4], a method that was verified by comparing with both well-known liquids (independent from those used for the calibration) and simulation models. This work investigates and characterizes an expansion of this numerical model which can extract, instead of just a bulk material spectrum, refined dielectric spectra of multiple stacked material layers, paving the way for dielectric spectrum analysis of stratified OoC models. The model's performance was benchmarked by measuring a multi-layer structure as a single bulk material and comparing the experimental spectrum to that computed by the numerical model. The data show an excellent match for the full range of heights, with a mean complex permittivity error of 2.42% (σ=1.35%) over 118500 datapoints of 3 differently sized probes, used in a field frequency range between 0.05 to 20GHz. This proves that the numerical model can fully capture the experimental data and can be used for multi-layer dielectric permittivity extraction, for which accuracy across depth is essential. In follow-up work, spectrum extraction of specific layers in stratified samples will be benchmarked. It would consist of three parallel measurements of the same analyte (Fig. 2): a reference, in direct contact with the analyte, and two multi-layer conditions, one with an interposed elastomer (poly-dimethyl siloxane (PDMS)) and one with PDMS and glass. The latter are common structural layers in OoC devices, whose characterization will aid in future non-invasive experiments with tissues.





Copper nanoparticle sintering enabled hermetic packaging with fine sealing ring for MEMS application

Ahmed Abdelwahab, Henk van Zeijl, Massimo Mastrangeli

Driving by the increased demand for hermetic packaging in the ‘More than Moore’ roadmap, a Cu nanoparticle sintering-enabled hermetic sealing solution was developed with a small-size sealing ring. The developed technology simplifies microfabrication and requires less surface roughness using a sinterable Cu nanoparticle paste. A 50 µm size Cu paste sealing ring was achieved using a lithography patterned photoresist as a stencil mask, as shown in Fig.1. A groove-structured chip was used to amplify localized stress. The Cu nanoparticle paste was fully sintered at 300 °C under pressure ranging from 10 MPa to 40 MPa resulting in a robust bonding with a maximum shear strength of 280 MPa (Fig. 2) and implementing hermetic packaging (Fig. 3). The deflection of the Si diaphragms estimated a vacuum level of 7 kPa. Figure 4 presents that vacuum sealing was maintained for over six months, and the lowest leak rate was calculated as 8.4×10-12 mbar/Ls. The developed technology that comprises small-size patterning and pressure-assisted sintering offers the potential for a simple, cost-effective, but robust solution for hermetic packaging.

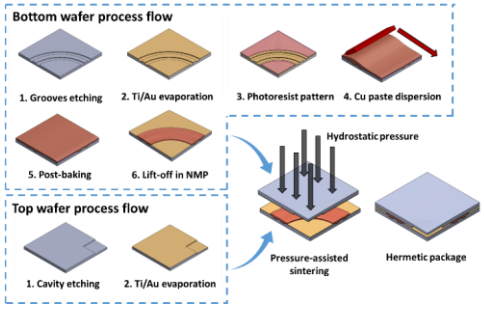


Figure 1. Microfabrication process flow (one quadrant of the die is presented for better illustration)

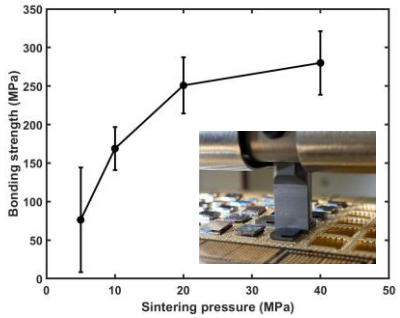


Figure 2. Bonding strength with different sintering pressure

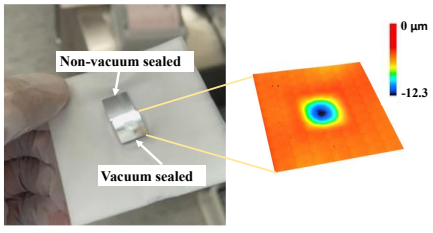


Figure 3. Sample sintered at 300 °C under 10 MPa and top surface 3D visualization.

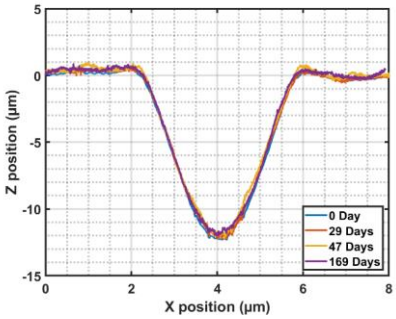


Figure 4. Evolution of the diaphragm deflection in the sample sintered under 10 MPa over 169 days.

Surface Acoustic Wave-based Sensor Design for CD9 Biomarker Detection to aid in Prostate Cancer Diagnosis

Johan W.D. Meyer

Among men, prostate cancer is the most diagnosed cancer. Luckily, blood serum prostate-specific antigen testing is very sensitive for prostate cancer. However, it is not very specific as it is also sensitive to benign hyperplasia. For this reason, actual diagnosis for prostate cancer can eventually only be done by biopsy. A procedure that is very uncomfortable for the patient and has high risks for conditions such as dysuria and haematuria. A more specific and risk-free diagnosis method is to investigate more accessible and specific biomarkers such as urinary-CD9. And these biomarkers should be easy and quickly detectable to enable large scale testing for early prostate cancer diagnosis.

Now, sensing for biomarkers is typically done using optical techniques which are time consuming and expensive. A sensor based on surface acoustic waves could prove a sensitive, cheaper and easier to use alternative.

The aim of this research is to design and fabricate a cheap and robust, sensor for CD9 detection using a love mode surface acoustic wave device operating at high frequency (near 500MHz) for the best achievable sensitivity.

Using finite element method simulations, the optimal surface acoustic wave device design is structurally determined. Then a fabrication process is designed to enable easy and straightforward fabrication of the sensor. Next, the optimal sensor layout is confirmed in physical measurements. Finally, the optimal surface acoustic wave device is mounted on a PCB and biochemically functionalised to detect urinary-CD9 in liquid samples using a vector network analyser.

It is expected the sensor will be able to detect CD9 in liquid samples with high sensitivity. By the use of antibody immobilisation, the sensor is also very specific for CD9.

Surface acoustic wave devices have been researched for many years now and are widely commercially applied. The use in biosensing for rapid point of care testing is a currently relevant application. It poses to be a robust, cheap and sensitive sensing mechanism.

Design and Simulation of a 6-bit SAR ADC with a Novel 2 µm SiC CMOS Platform for Extreme Environment Applications

Yunfan Niu, Jiarui Mo, Sten Vollebregt, Alexander May, Guoqi Zhang

In this work, a 6-bit Successive Approximation Register Analog-to-Digital Converter (SAR ADC) was designed and simulated utilizing state-of-the-art 2 µm Silicon Carbide (SiC) Complementary Metal-Oxide-Semiconductor (CMOS) technology, targeting harsh-environment applications. The motivation behind this research arises from the increasing demand for electronic components that can reliably function under extreme environments where Si electronics cannot. The simulation result shows that the SiC SAR ADC is able to operate within a wide temperature range from 150 to 300°C and achieves a sample rate of at least 1.25kHz. The design exhibits good linearity, with a Differential Nonlinearity (DNL) ranging from -0.21 to 0.31 LSB, and an Integral Nonlinearity (INL) peaking at 1.03 LSB. The layout of the ADC has been carried out with a process design kit provided by FhG IISB, resulting in a chip size of 4.85mm by 4.85mm, including logic gates, buffers, and capacitors. Future work includes measuring the 6-bit SAR ADC under real-world hazardous conditions to verify its resilience and robustness, which will further validate the merits of SiC CMOS technology in extreme environments.

Pyramid-Shaped 3D Hall Sensors

Jannik Strube, Jacopo Ruggeri, Karen M. Dowling

This new PhD project aims to realize a new kind of 3D Hall sensor, based on an inverted pyramid structure. With the proposed design we seek to overcome the limitations of state-of-the-art Hall magnetometers and introduce a novel sensor platform that enhances the performance of silicon-based devices and opens new pathways for the utilization of alternative materials in single-chip 3D Hall sensors for the first time.

Instead of three separate devices, one for each of the magnetic field components, the sensor features only a single active area to sense spatial fields, reducing the overall layout complexity and size. Initial simulations suggest that identical sensitivities for in-plane/out-of-plane modes can be achieved by tuning cavity-to-contact size ratios. The structure is created by anisotropic etching of (100) silicon to expose 54.74°-sloped (111) sidewalls, which additionally function as natural etch stop, assuring high accuracy and reproducibility. The first project stages include iterative simulation, design, manufacturing, and characterization of silicon-based devices, leveraging the Else Koi Laboratory's CMOS processing line at Delft University of Technology to create fully integrated sensors.

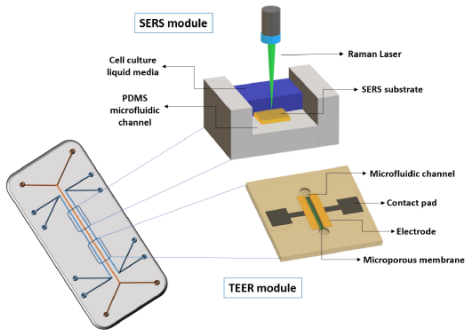
In parallel, the deposition of alternative materials as active layer is explored. Special interest lies in high-mobility and high-bandgap materials, such as graphene, diamond, GaAs, 2DEG-heterostructures, SiGe, InP, or cubic BAs. Some materials have been already proven to work as Hall sensors: 2DEG-heterostructures utilize film stress in layer stacks of piezoelectric semiconductors to create a two-dimensional electron gas (2DEG) with high carrier mobility and wide temperature operation range; single-layer graphene exhibits high Hall-sensitivity and very low detection limits; and GaAs sensors are already commercially available, manufactured from mono-crystalline substrates. The main challenge for the application of alternative materials is to create high-quality films inside the etched cavity. The crystalline Si (111) surfaces in general can promote crystalline film growth, but good film integrity over the corners, thickness uniformity and a high degree of crystallinity are required to create high-sensitivity devices.

The proposed 3D Hall sensor platform can be applied in various fields, e.g. enabling tactile sensing in industrial robotics, magnetic field mapping of permanent magnets, or navigation of surgery equipment in endovascular procedures. With the pyramid structure offering high sensitivity ratios between the different field components, precision spatial position sensing is available with simple device integration. Utilization of non-silicon active layer materials allows to tune specific device parameters to the application requirements, for example to achieve low detection limits in geomagnetic navigation systems or robust sensors for harsh environments.

Integrated sensing for biomolecular and barrier integrity analysis in organ-on-chip systems

Pratik Tawade, Massimo Mastrangeli

Organs-on-chip (OoCs) are in-vitro systems that recapitulate in-vivo-like tissue and organ functions to provide more realistic mimics of human physiology and disease than existing in-vitro models. OoC technology may accordingly screen the toxicity and efficacy of drugs with higher effectiveness and reliability. OoCs can be used for drug development to assess the effects of drugs on human tissues, in personalized medicine to evaluate the proper drug and dosage for a patient, and for developing disease models to study mechanisms and potential therapies [1]. Monitoring the OoC microenvironment and the dynamic response of the miniaturized organs is thereby critical. Particularly, there is an increased need of integrated sensors which provide continuous real-time in-situ measurements.To address these unmet needs, this work investigates the possibility of in-line surface-enhanced Raman scattering (SERS) for detecting cell culture components in a microfluidic OoC system, as well as integrated impedance sensing for tissue barrier monitoring. SERS is a sensitive tool for investigating cell-specific responses to activation stimuli and monitoring subcellular molecular changes [2]. We are developing SERS technology to detect and study biological components of cell culture media such as cytokines and chemokines, which are small proteins crucial in controlling the activity of immune system cells. Moreover, culture models of biological barriers, such as intestinal, are essential for studying pathophysiological functions, drug adsorption, and disease mechanisms [3]. Measurements of trans-epithelial electrical resistance (TEER), and impedance spectroscopy more generally, offer invaluable insight into how tissue barrier disruption causes ailments like inflammatory bowel disease, including Crohn's disease and ulcerative colitis. Impedance spectroscopy across a cellular monolayer quantifies the permeability and integrity of tight junctions formed by barrier cells. We are designing a novel silicon-based OoC device for measuring intestinal barrier permeability using impedance spectroscopy. The device features integrated electrodes and a microporous membrane enabling an in-vivo-like separation between cells which aids in establishing realistic in-vitro gut models. Integration of SERS and TEER sensors within microfluidic OoCs will significantly expand their functionality, and enable further tailoring of the devices to fit a wider range of (patho)physiological models.



Integration of SERS and TEER in a single microfluidic organ-on-chip device will allow in vitro biomolecular detection of vital components and monitor tissue barrier function in real –time

Laser Pyrolysis Direct Writing for Rapid Fabrication of High-Performance Flexible Pressure Sensors with Micro-Truncated Pyramid Array

Shaogang Wang, Qihang Zong, Huiru Yang, Chunjian Tan, Qianming, Huang, Xu Liu, Guoqi Zhang, Huaiyu Ye, Paddy French

Developing flexible pressure sensors that are low-cost, scalable, and easy to fabricate is crucial for advancing flexible electronics, particularly for high-performance sensors that require precise surface microstructures. However, optimizing complex fabrication processes or using expensive microfabrication methods remains a significant challenge. In this study, we introduce a laser pyrolysis direct writing technology that allows for efficient and rapid fabrication of high-performance flexible pressure sensors with a micro-truncated pyramid array. The pressure sensor exhibits high sensitivity (3132.0 kPa-1, 322.5 kPa-1, and 27.8 kPa-1) in pressure ranges of 0-0.5 kPa, 0.5-3.5 kPa, and 3.5-10 kPa, respectively. Additionally, it has a fast response time (22 ms for loading and 18 ms for unloading) and high reliability over 3000 pressure loading and unloading cycles. The pressure sensor can also be easily integrated into a sensor array to detect spatial pressure distribution. The laser pyrolysis direct writing technology introduced in this study presents a novel and promising approach to designing and fabricating high-performance flexible pressure sensors using micro-structured polymer substrates.

Inductively coupled plasma deep reactive ion etching of high aspect ratio structures on 4H-SiC for MEMS applications

Zhenhua Zhang, Jiarui Mo, Sten Vollebregt, Karen Dowling, GuoQi Zhang

An inductively coupled plasma deep reactive ions etching (DRIE) process was developed for 4H-SiC based on MEMS applications using SF6/O2 gases. Die-level samples were etched at different process conditions, such as ICP source power, platen power, gas flow, and carrier wafer materials. The nickel (Ni) layer was applied as a hard mask for SiC etching.

Initial SiC etching tests were performed using the sapphire carrier wafer due to the good etch selectivity over SiC samples. However, a massive micro-masking effect was observed, where the etching surface was covered with pillars. According to energy-dispersive (EDS) spectroscopy analysis, the pillar consists mainly of aluminum (Al). This indicates that the pillar is most probably induced by the re-deposition of Al from the carrier wafer during ion bombardment. After doing plasma pre-treatment on the sample, the micro-masking effect was significantly suppressed. We found the micro-masking effect can be further eliminated by replacing the sapphire carrier wafer with the Si wafer at the cost of etch selectivity over SiC samples. The preliminary result also shows that the etch rate can be significantly improved by applying higher platen power. Currently, the maximum etch rate is 1.1 um/min with a nickel hard mask selectivity of over 50 when the platen power is 300 W.

A comprehensive design of experiments (DOE) will be performed soon to understand the effect of each process parameter. In addition, high-temperature etching and cryo-etching are planned.

Piezoelectric Micromachined Ultrasound Transducer (PMUT) Based on Lithium Niobate – Design and Modelling

Xiaoxi Zhao, Michiel Pertijs, Tomás Manzaneque

Micromachined ultrasound transducers are found in many applications, such as medical imaging and intrabody communication. Piezoelectric micromachined ultrasound transducers (PMUTs) offer advantages over capacitive micromachined ultrasound transducers (CMUTs) due to their wider linear displacement range and the absence of bias voltage requirements. Moreover, PMUTs address limitations associated with bulk piezoelectric transducers, such as high acoustic impedance mismatch and incompatibility with CMOS technology. State-of-the-art PMUTs, based on aluminum nitride (AlN), suffer from low transduction efficiency, due to the moderate piezoelectric coefficients of AlN. In this work, we propose the use of lithium niobate (LiNbO3 or simply LN) for building PMUTs. LN is a single-crystal material with piezoelectric coefficients about one order of magnitude above those of AlN. Moreover, LN exhibits a strong in-plane piezoelectric coefficient, $e11$, which enables the construction of PMUTs with strong transduction, only using top-side electrodes with alternating polarity. Our LN PMUT concept, illustrated in Fig.1, is composed of two pairs of electrodes on the top of a suspended film stack with LiNbO3 and SiO2 on the top of a silicon wafer. By employing alternating electric fields, opposite stress directions are generated, as depicted in Fig.1, generating bending moment in the film stack. The optimal device design is such that the electric field is oriented at 30° with respect to the main polarization axis (Z) of an X-cut LN film.

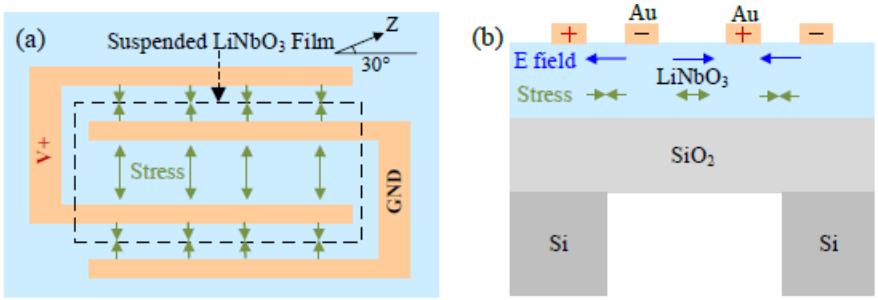


Fig. 1. (a) Top and (b) cross-sectional views of the lateral field $LiNbO_3$ PMUT. In (a), the dashed box depicts the released region Z indicates the main polarization axis of the X-cut $LiNbO_3$ film.

Nervous systems-on-Chip: An enabling medical device technology

Rahman Sabahi-Kaviani, Suzanne Timmermans, Gülden Akcay, Regina Luttge

Nervous system-on-Chips (NoC) are promising microfluidic models for furthering our understanding of neurodegenerative diseases and their potential therapeutic interventions. Of particular interest is the use of these chips for studying the effects of mechanical and geometric cues on neuronal cell cultures. In line with this, we have previously demonstrated that so-called actuator chips can be employed to exert nanoscale mechanical loads on cortical networks derived from rat primary cells by microfluidic pneumatic deformation of a polydimethylsiloxane (PDMS) membrane. Furthermore, we have demonstrated that microscale tunnels can be used to guide axonal growths of SH-SY5Y neuroblastoma cells.3 In this study, we introduce NoC as an enabling medical device technology to control the development of neural networks. We employ soft-lithography to fabricate PDMS chips with microliter-size cell culture compartments that can be connected using microfluidics assemblies with different substrate materials all uniquely influencing the cell culture performance. Hence, our NoC assemblies might enable medical device technology for studying the responses of healthy versus diseased neuronal cell networks in future applications.

ENABLING LONG-TERM LIQUID HANDLING IN DIGITAL MICROFLUIDICS PLATFORMS FOR CELL CULTURE SETTINGS

Oksana K. Savchak, Burcu Gumuscu Sefunc

Digital microfluidics (DMF) platforms have garnered increasing attention over the past decade thanks to its ability to address individual droplets. Programmed sub-microliter scale droplets performing basic pipetting operations paved the way for the automation of laborious assays 1. Automated biological assays are an exciting application of DMF, including DNA-based analysis 2, electroanalysis 3 and short-term cell culture experiments 4. However, DMF chips are not yet able to withstand long-term cell studies due to high humidity (95%) conditions in typical cell-culture incubators, as the aqueous content leaks in between the layers of the chips. This results in current leakage and compromises the accuracy of the assay. This reveals a new challenge, how to incorporate more complex cellular studies onto the platform. In this study, we propose and demonstrate a new fabrication process where i) the use of photoresist as dielectric material creates a water-impenetrable barrier, ii) the combination of a second dielectric material prevents degradation and current leakage of the material at high voltages (Figure 1). The DMF chip was fabricated using the DropBot prototype with SU-8 3005 and Polyvinylidene fluoride (PVDF) as dielectric layers. SU-8 3005 has a thickness of 5 µm and was processed according to the manufacturer's instructions. PVDF underwent evaporation at 60°C for 1h and baking at 180 °C for 30 min to promote β-phase formation 5. Surface properties were characterized using white light interferometry and dielectric constant was measured using impedance spectroscopy. Material stability to working range voltages (0-200 V) was assessed via voltage-current curves. Actuation voltage was determined through water contact angle measurement. Water penetration assay was conducted by storing chips with 20 µL droplets in a 95% humid environment and 37 °C, while measuring current output at correspondent spots every 24 hours over 7 days. SU-8 remained hydrophobic over time and has a dielectric constant of 4.5. Nevertheless, it does not tolerate high-voltage applications, leaking current at ~140 V. On the other hand, PVDF has a higher dielectric constant of 12.58 and a smoother surface. However, it is incompatible with cell culturing as it shows high current flow (100 µA) at voltages necessary for droplet actuation (70 V). Dielectric stacks consisting of these two materials enabled a stable dielectric layer (<20 nA current) when applying high voltages (200 V). To study the water penetration into the dielectric, the above-described samples were compared to 6 µm-thick Parylene C, which is typically used in commercial chips. While it showed breakdown and current leakage, reaching almost 100 mA in 24h, samples containing SU-8 as a dielectric layer resulted in stable performance and insignificant nA-level current leakage over 7 days. Our work showcases the feasibility of adapting digital microfluidics to long-term cell studies that were previously deemed unsuitable. Our strategy opens the possibility of developing on-chip cell cultures with semi-automated media supplementation with a minimum duration of 7 days while maintaining the integrity of the chip. This approach further enables the use of the chip for subsequent assays, without any compromise to its functionality.

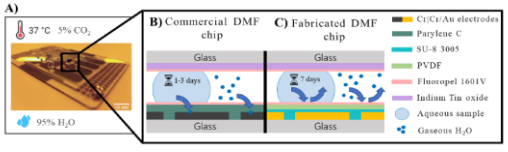


Figure 1: DMF chip response to cell-culture conditions. A) An image of an in-house fabricated DMF chip placed at 37°C, and 95% humidity conditions with a droplet on the surface. B) In cell-culture conditions, a commercial chip with Parylene C as the dielectric layer results in water penetration and chip degradation in 1-3 days. C) In cell-culture conditions, our DMF chip with dielectric stack prevents water penetration and chip degradation over 7 days.

Characterization of Photodiodes in 22 nm FDSOI at 850 nm

Jelle Bakker, Mark Oude Alink, Jurriaan Schmitz, Bram Nauta

We present the analysis and measurement results of photodiodes (PDs) fabricated in 22nm Fully-Depleted Silicon-On-Insulator (FDSOI) technology at a wavelength of 850nm. To the best of our knowledge this is the first paper to give detailed information about PDs in 22nm FDSOI. FDSOI has the unique opportunity to place a PD in SOI, which is potentially very fast, on top of bulk devices such as PNP-transistors for temperature sensors. Its measured responsivity is 4 µA/W at a bandwidth (BW) of 3.4GHz. Several bulk PDs, including PW/NW/DNW, PW/DNW/PSUB, and NW/PSUB have also been characterised. They have responsivities between 6mA/W and 207mA/W and BWs between 23MHz and 5.8GHz. 22nm FDSOI shows potential for fully-integrated high-speed optical receivers, as it combines ∼90nm bulk CMOS PD performance with 22nm RF and digital processing capabilities on a single die.

A 50µW 2.45GHz Direct-Conversion RX with On-Chip LO with -84dBm Sensitivity for 1Mb/s GFSK

Maryam Dodangeh, Mark S. Oude Alink, Jan Prummel, Bram Nauta

In this paper, an ultra-low-power 2.45GHz mixer-first low-IF receiver front-end is presented. To have extremely low power consumption, a technique for implementing an on-chip low-power local oscillator is proposed that contains a 9-stage pseudo-differential ring oscillator operating at 1/9 of the RF frequency. As well as reducing the power consumption, this technique results in having a lower 1/f3 phase noise corner frequency. The proposed front-end is fabricated in GF22nm FDSOI technology. It consumes 50µW and has 2x less power than the state-of-the-art while having competitive calculated sensitivity of -84dBm for 1MHz GFSK demodulation.

Extremely low power consumption of 50µW is achieved by 1) avoiding gain at RF by having a mixer-first RX, 2) having a ring oscillator (RO) operating at 9x lower frequency than fRF (fRO=fRF/9), 3) introducing an edge-combiner (EC) circuit to have 3x frequency multiplication and generate proper phase differences for a 3-path differential mixer, and 4) using the 3rd harmonic of the LO for down-conversion with a 3-path mixer to achieve input matching with small mixer switch size. These design choices enable us to have the minimum possible transistor size (80nm/20nm in GF22nm) for the RO, ECs, and LO buffers for a record low power consumption that may further scale with technology.

Bluetooth Backscattering – Phase noise measurements

Erwin Hardeveld, Jeffrey Stroet, Ronan van der Zee, Bram Nauta

A way to radically decrease power consumption in wireless sensors is to use backscatter communication. Instead of actively transmitting RF power, a carrier signal is reflected at the antenna. This carrier signal is provided from the reader device, which has a higher power budget. This technique omits all RF circuitry at the wireless sensor. Existing backscatter tags need specialized reader hardware to generate the carrier and read out responses. Alternatively, research has shown that existing modulation standards like Bluetooth can be used such that commodity receivers can be used for reception. This work presents measurements done to determine the phase noise requirement of a backscatter tags to achieve reliable communication. Using these results, a backscatter tag with minimum power consumption can be designed.

High-speed ADCs for communication applications

Josef Heel, Harijot Singh Bindra, Bram Nauta

In the area of high-speed radio communication, RF direct-sampling receivers are gaining more attention. This work focusses on a time-interleaved Nyquist ADC in 22nm FDSOI operating at 10-20GS/s. Pushing the analog input bandwidth to as high as possible while maintaining sufficient linearity enables direct-sampling applications up to microwave frequencies, but puts stringent demands on the input stage. Particularly, the realization of a track-and-hold requires new topologies and careful optimization of the input structure.

A Single-Trim Frequency Reference System with 0.7 ppm/°C from −63 °C to 165 °C Consuming 210 µW at 70 MHz

Delke, A. S., 1 Hoen, T. J., Annema, A. J., Jin, Y., Verlinden, J., & Nauta, B.

This poster presents a frequency reference system that combines high frequency accuracy and low power consumption using a single-point temperature trim and batch calibration. The system is intended as a low-cost fully integrated crystal oscillator replacement. In this system, the oscillation frequency of a power-efficient, but Process, Voltage, Temperature (PVT) and Lifetime (L) sensitive current-controlled ring oscillator (CCO) is periodically (re)calibrated by the well-behaved frequency stability of an untuned LC-based Colpitts oscillator (LCO), which is optimized for stability over PVTL. During the single-point room temperature factory trim, the frequency of the LCO is determined and the result is digitally stored. An on-chip calibration engine tunes the ring oscillator to the target frequency based on the LCO frequency, temperature sensor information and digitally stored trimming information, thus effectively improving the frequency stability of the ring oscillator. The relatively high-power LCO is heavily duty-cycled to minimize the overall power consumption. A prototype fabricated in a 0.13 µm high-voltage (HV) CMOS SOI process and assembled in a plastic package demonstrates an inaccuracy lower than ±93 ppm over a temperature range from −63 to 165 °C across 18 samples. The presented frequency reference system, including on-chip voltage regulators and a temperature sensor, occupies a chip area of 0.69 mm2 and consumes about 64 µA from a single 3.3 V supply. The frequency error due to supply variation is roughly 92 ppm/V. The mean frequency shift due to aging, measured before and after a six-day storage bake at 175 °C, is only 52 ppm.

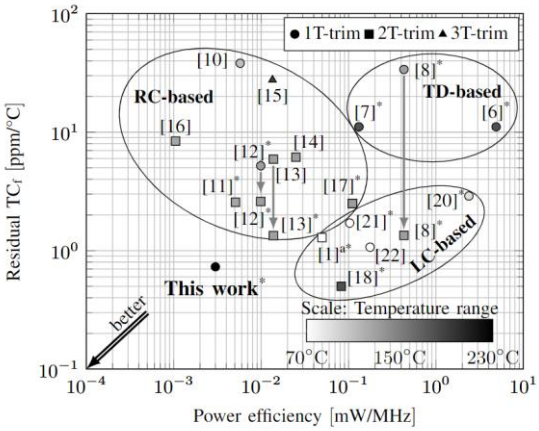


Figure 1. Overview of prior art fully-integrated frequency references as a function of power efficiency and residual TC_f after trimming. Oscillators are grouped by type (RC-based, TD-based, LC-based). The marker type indicates the number of factory temperature trimming points (● 1T-trim, ■ 2T-trim, ▲ 3T-trim) and the marker color indicates the reported temperature range. Aging effects are not included. [a]2T-trim, see [28]. *With batch calibration.

Multiple Output Clock Synthesis using Fractional Output Dividers & Digital-to-Time Converters (DTCs)

Nimit Jain, Eric Klumperink, Bram Nauta

Modern electronic systems-on-chips (SOCs) are heterogenous blocks consisting of various modules to support a vast range of functionalities: digital, analog, mixed signal and radio frequency (RF). Each module requires a clock at a certain frequency to achieve the most optimized performance [1]. The clocking circuitry therefore needs to cater to the various requirements of each module. The performance requirements from this clock circuitry are becoming increasingly stringent: generation of vast range of output frequencies with high frequency resolution, low spurious tones, low root mean square (RMS) jitter, low area occupation and low power consumption. To meet these requirements, the fractional-N phase locked loops (FNPLLs) based approaches are no longer sufficient. Alternatives to FNPLLs are Fractional Output Dividers (FODs) which consume lower power and area, barely interact with other blocks, and can instantaneously switch from one frequency to another. However, they generate a lot of spurs in their frequency spectrum. The goal of our research is to reduce these spurs using digital-to-time converters (DTCs).

Hardware Implementations for Voice Activity Detection: Trends, Challenges and Outlook

Patrice Abbie D. Legaspi, M.Sc., Shubham Yadav, M.Sc., dr. ir. M.S. Oude Alink, dr. ir. A.B.J. Kokkeler, prof. dr. ir. B. Nauta

Voice Activity Detection (VAD) is a technique used to identify the presence of human voice in an audio signal. It is implemented as an always-on component in most speech processing applications. As speech is absent most of the time, this component typically dominates the overall average power consumption of the system (excluding microphone). The widespread usage in speech applications and the need for ultra-low power VAD have led to a plethora of algorithms and implementations in the hardware domain, necessitating a comprehensive study and analysis to identify design trends, challenges and guidelines for future implementations and testing of VAD devices.

A scoping review was conducted to identify the articles for hardware implementations of VAD from January 2010 - December 2021. The results highlight a big design space being used for VAD along with a lack of standard testing methodology and usage of application-dependent performance metrics. An increased usage of filter-based feature extractors along with neural-network-based classifiers is observed. Due to lack of standardization, no other trends can be established from the results. Thus, a set of rules and guidelines are provided to facilitate the future development and benchmarking of VADs.

Logic families for frequency dividers

Klaas de Haan, Robin Lohuis

Frequency dividers can be constructed using flip-flops, which are fundamental building blocks for sequential logic circuits. Flip-flops can be implemented using different logic styles, each offering its own advantages and trade-offs [1]. Common logic styles used for flip-flops include CMOS, CML (Current Mode Logic), TSPC (True Single-Phase Clock) and C²MOS (Clocked CMOS).

CMOS SR-latches are known for their low power consumption due to their minimal transistor count. They employ a regenerative latch structure, allowing for no minimum clock speed and providing a full swing of the output. However, CMOS latches have the drawback of high dynamic power dissipation due to the presence of numerous transistors, especially when combining logic gates to reduce the transistor count.

CML is a logic type that operates based on current signals rather than voltage. It offers advantages such as high-speed operation and reduced noise susceptibility. CML flip-flops use differential pairs of transistors to achieve current-mode switching, enabling efficient frequency division. Because these current sources are continuously active, the static power consumption of this logic type is high.

TSPC logic employs a single-phase clock signal and offers improved speed and reduced power consumption compared to traditional flip-flops [2]. TSPC flip-flops use a precharge phase and an evaluation phase, allowing for efficient storage and propagation of data [3]. Because these phases are implemented in physically distinct stages, these flipflops require more stages than C(²)MOS and have a larger propagation delay. These flip-flops require careful sizing of transistors to ensure proper functionality and timing. TSPC does not need complementary input signals and does not provide complementary outputs.

C²MOS integrates transmission gates into inverters, resulting in clocked inverters. These clocked transistors can be on the inside or the outside of the inverters, trading charge sharing effects for speed [4]. The inverter precharges the internal nodes while the clock transistors strobe the logic level to this output. C²MOS requires a complementary clock and higher supply voltages for stacked transistors.

In summary, CMOS offers a regenerative latch structure and wide output swing, but it consumes more power due to a higher transistor count. CML operates based on current signals, providing advantages such as high-speed operation, but have high static power consumption. TSPC logic offers improved speed and power efficiency with a single-phase clock but requires more stages and therefore has a larger propagation delay. C²MOS also offers speed and power efficiency by precharging internal nodes and solves the slower propagation delay of TSPC at the cost of a complementary clock requirement and higher supply voltages. Understanding the characteristics and trade-offs of these logic types is essential for designing efficient frequency dividers.

Efficient Analog-to-Feature Extraction for Low Power Keyword Spotting Applications

A.K. Rajendra, H.S. Bindra, B. Nauta

Traditional Keyword Spotting (KWS) systems utilize fully digital Feature Extraction (FEx), where the Analog-to-Digital converter (ADC) captures samples and a Digital Signal Processing (DSP) block processes them in the frequency domain. However, in mixed-signal applications like KWS, the overall system performance can be limited by the capabilities of the ADC. While ADCs have made significant performance advancements over the years, reaching near-theoretical limits, it remains a considerable challenge to surpass these limits using conventional ADC methods.

To address this challenge, application-aware ADCs leverage prior knowledge about the incoming signal. This is because the bandwidth of the extracted features is significantly lower than the true physical bandwidth of the signal. By applying analog processing techniques, it becomes feasible to reduce the physical bandwidth of the signal to closely match the feature bandwidth. Subsequently, the signal can be sampled below its true Nyquist rate, resulting in improved efficiency and cost-effectiveness.

Digital Harmonic Rejection in N-Path Filters

Stef van Zanten, Jeroen Ponte

N-path filters are desirable for use in radio receivers due to their programmable center frequency and high Q. Unfortunately, due to their discrete-time nature, they display harmonic responses. A number (depending on the number of paths N) of these harmonic responses can be nulled by applying a technique known as Harmonic Rejection (HR). HR relies on first accurately weighting the signals in each of the N-path filters paths and then recombining them. This weighting is typically performed in the analog domain, where finite implementation accuracy (due to e.g. mismatch) decreases the depth of the notches, thus degrading the HR.

In this work, we aim to instead implement the HR weights in the digital domain. This theoretically allows for arbitrarily high weight accuracies, which should yield arbitrarily deep notches. However, bringing the analog N-path signals into the digital domain requires an ADC. Practical ADCs, with their finite resolution, introduce errors which may also degrade HR notch depth. A main research focus of this work is to investigate the impact of finite ADC resolution on the efficacy of a digital HR N-path filter signal chain in which it is applied.

Improved Toolchain-Compatible Standard Cells with 5% - 36% Lower EDP for Super Threshold Operation in 65nm Low-Power CMOS Technology

S. Yadav, A.B.J. Kokkeler & M.S. Oude Alink

High performance and energy efficiency are very crucial aspects in e.g. the field of edge computing where a tight power budget constrains the device operation. Different logic families were explored over the years to design standard cells with higher performance and/or lower power while keeping the noise immunity and the compatibility with design automation tools intact. Hybrid pass transistor logic with static CMOS output (HPSC) seems to be promising and is exploited in this paper to design low energy, high performance and toolchain-compatible standard cells without compromising on noise immunity and chip area. This paper presents a 2/3-input XOR cell, a 2/3-input XNOR cell, two variants of a half adder cell, a full adder cell and two variants of a 1-bit multiply-accumulate combinational cell based on a combination of HPSC and static CMOS logic in a commercial 65nm Low-Power CMOS technology. Post-layout simulations over all the process-voltage-temperature corners show a 4.7% - 35.7% lower energy-delay product with significant improvement in the propagation delay of the proposed cells.

High Risk No gain – Limitations of bottom-plate NPath mixer-first receivers

Emiel Zijlma, Roel Plompen, Eric Klumperink, Bram Nauta

N-path filter/mixers play an important role in the enabling of software defined radio. The N-path filtering characteristic attenuate out-of-band blockers, allowing for an interference-robust receiver. The radio frequency (RF) range of N-path filters are tuneable by adjusting the clock frequency. N-path bottom-plate switches are used to improve the N-path linearity compared to the more conventional top-plate switch design. However, the parasitic shunt capacitances at the RF-node introduce signal losses and noise figure degradation. This effect is more severe at higher radio frequencies, limiting the practical tuning range of N-path filters to roughly 2GHz. This project explores techniques to mitigate the N-path performance degradation due to the RF-capacitances. Tackling this will be a major step towards fully integrated receivers.

Mm-wave RFIC Designs

Kaijie Ding, Johan Holmstedt

Recently, several interesting applications for integrated systems at millimeter-wave (mm-wave) frequencies have emerged, such as automotive radar, wireless communication, sub-THZ spectroscopy and imaging systems. The primary driving force behind the shift towards higher frequencies is the abundant bandwidth available in the mm-wave spectrum. The additional bandwidth offers significant advantages in terms of achieving higher data rates in communication system and enhanced distance resolution and angular resolution in radar applications.

Moreover, the compact size of mm-wave antennas enables the implementation of massive MIMO and beamforming techniques. These advancements have the potential to substantially increase channel capacity and improve overall performance. However, the shift towards higher frequency also brings challenges in RFIC designs.

One of the challenges encountered in mm-wave systems is to achieve high PA/TX efficiency. Operating at mm-wave frequencies often imposes constraints on the power, gain and matching. Also, the accuracy of the simulation and modeling play an important role in the final performance.

Another significant challenge in mm-wave systems lies in the distribution of the Local Oscillator (LO) signal. Distributing high-frequency signals on chip at higher frequencies lead to increasingly high losses.

Addressing these circuit challenges in mm-wave systems requires a combination of innovative circuit design, advanced integration techniques, and careful system-level considerations. As part of these efforts, serval RFIC chips operating between 20 GHz and 140 GHz are tape-outed and measured. These chips focus on RF beamforming and high efficiency transmitters at 20-70 GHz for communication, and D-Band radar transceivers for sensing and automotive application.

AI-assisted design verification of High-Performance Mixed Signal Systems

Stijn Ringeling

Integrated Circuit validation simulations are important to ensure the circuits achieve the target performance with the required statistical coverage. However, simulation times are increasingly longer as the circuits upscale. In the case of complex Delta Sigma Modulators (DSMs) it can take up to 4 weeks to validate one design point. In this project the possibility of using machine learning to reduce the required validation time is explored. Currently, methods exist that can learn from example circuits to predict varying performance metrics as well as synthesize entirely new circuits. However, these methods have not been applied to complex circuits such as the DSM. Furthermore, the training of Machine Learning models requires large amounts of data, which is a time intensive task to generate. In this research we hope to overcome these problems as well as explore multiple Machine Learning application to the world of Integrated Circuit verification.

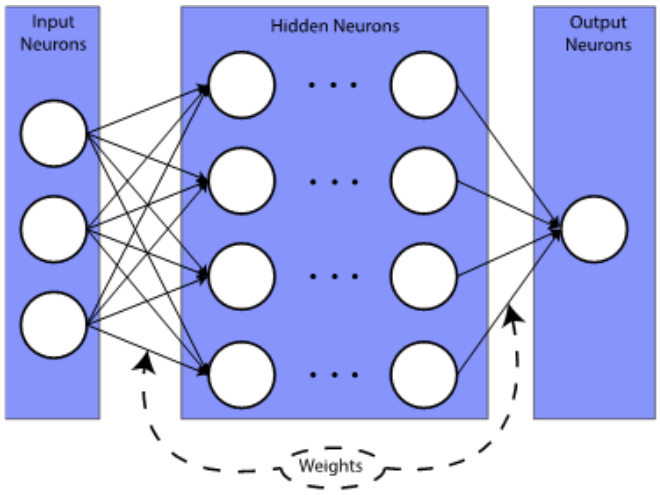


Fig 1: Overview of a general Machine Learning model

Electronics-based Terahertz Sensors in Agriculture

Maryem Tanveer, Piyush Kaul, Marion K. Matters-Kammerer

This work is part of the SYNERGIA project that involves development of the concept of technology-4-ecology-base farming. Presently, research in agriculture (e.g. crop/animal science) has focused on increasing the productivity of conventional homogeneous systems mainly through optimizing external inputs. However, the sustainable functioning of these systems critically depends on understanding biological processes that autonomously drive performance and stability. Thus, the adoption of ecology-based systems is hampered by the fact that their complexity makes their management and control difficult, labor-intensive, and costly, and the appropriate technology is currently not well-developed.

This work involves research toward sub-terahertz spectroscopic imaging of plants. On the surface of leaves, the diseases change the reflection and transmission properties in the sub-terahertz frequency range. Therefore, based on new devices generating and receiving sharp pulses (ultra-broadband spectrum), the amplitude and phase response of the plant will be analyzed. This project will involve work on the development of an electronic imaging spectrometer for the detection of diseases of leaves in use cases, horticulture, and arable farming. The main objective of this research will be to develop a broadband sensor array at sub-terahertz frequencies, which could be utilized for different agricultural applications within and outside the scope of this project. Integrating the source-plant-detector system into silicon-based high-volume technology will be an enabler for high-volume manufacturing, enabling mainstream adaption of this work. The project focuses on high-frequency IC design and on demonstrator development, including the research of the optimized signal path.

As a first step, several lab-base spectroscopy methods will be tested to gain insight into the capabilities and limitations of such methods in addition to understanding the design challenges for electronics-based sensors. In this work, several characterization techniques (continuous-wave and pulsed) will be studied and explored to find the most optimal method for sensing using electronics-based sensors at Terahertz frequencies. As a step toward electronics implementation, a pulsed-source will be researched and implemented in silicon-based technology at sub-terahertz frequencies.

Integrated Circuits - Designed by the Public

Elles Raaijmakers MSc, Jelle Verest, prof. dr. ir. Peter Baltus

In 2020, the company Skywater released a PDK for designing 130 nm electronic chips. Accompanying software has been released as well, and a workflow from circuit design to layout generation using only free tools has been established. Google and Skywater even promised to produce well-designed chips that were submitted to them for free. For the first time, this enabled the interested hobbyist to design an IC by himself. In practice, however, this opportunity is primarily taken up by engineers that already work in chip design or closely related fields.

With the shortage of good designers in mind, we want to make chip design more accessible. But before the interested layman can give chip design a go, a few additional things beyond the open PDK and design flow are required.

First of all, the information on to how to design an (analog) IC using the free software is scarce. So for the past year, we have been working on setting up tutorials related to analog IC design. To that end, inexperienced students were asked to design a simple analog circuit and layout using the design flow. The problems that they encountered were closely monitored, and the designs that they made are currently reworked into a tutorial. Aside from providing information about the software tools, the tutorials are also intended to introduce some analog design strategies, such as small-signal analysis.

Secondly, the available information regarding IC design is mostly written in jargon. It takes time even for someone from a related field to translate everything and distinguish the relevant information from the irrelevant facts. Therefore, we have written an instruction manual. The manual contains explanations to where to download the software, how analog IC design processes work, which considerations there are when drawing a layout, what certain jargon terms mean, etc.

Lastly, some important information regarding analog design is lacking. Because the 130nm PDK is mainly digital design-oriented, basic analog design parameters such as the frequency limitations are currently unknown. We are therefore setting up a modeling study to gain insights regarding these limitations.

In the future, we hope to use the aforementioned tutorials, the instruction guide and the improved knowledge of the design parameters to bring IC design closer to the interested layman.

TOWARDS A GAS INDEPENDENT THERMAL FLOW METER

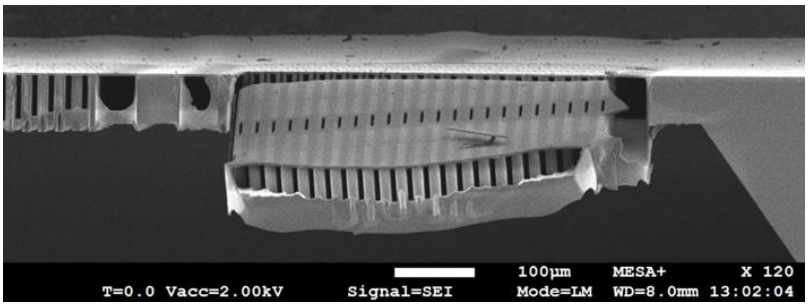
Shirin Azadi Kenari, Remco J. Wiegerink, Remco G.P. Sanders, and Joost C. Lotters

We present a novel gas-independent thermal flow sensor chip that contains three calorimetric flow sensors to measure the flow profile and flow direction inside a tube, and a flow-independent thermal conductivity sensor which detects the type of gas through a simple DC voltage measurement. Four different gases were used for the thermal conductivity measurement and the measured output voltage corresponds very well with a theoretical model.

Inline Micro-fluidic Relative Permittivity Sensor Based on Silicon Wafer Technology

M.J.S. Bonnema, D. Alveringh, H.-W. Veltkamp, R.J. Wiegerink

This work presents the design, fabrication, and characterisation of an inline micro-fluidic relative permittivity sensor based on silicon wafer technology. The need for the aforementioned sensor is large: in addition to the possibility of detecting and determining fluids based on one of their physical properties, it also enables further integration of micro-fluidic sensors. The design process of the sensor has been subject to multiple stages. The work discusses an overview of the relevant fundamental theories, both in the electrical and fluid domain, and reviews the Simplified Trench-Assisted Surface Channel Technology. The design of the micro-sensor is examined, and the choice for a parallel channel approach is explained. Finite element modelling is used to aid the design process. The simulated results are compared to those from the theoretical analysis, the results in the electrical domain correspond closely to theoretical values. However, the fluidic model could not be verified in this manner. Furthermore, five lithography masks have been designed and utilised in the fabrication process. The fabrication process is based on the Trench-Assisted Surface Channel Technology to obtain a true parallel electric field across the micro-channel. The process flow has been fully executed, realising a permittivity sensor with – among others – 29 parallel channels, each of 5 µm wide and approximately 60 µm deep. Fluidic connections are etched on either side of the sensor, and the sensor structure is released from the bulk via a potassium hydroxide etch. During the latter step, issues arose which damaged the metal layer. However, by exploiting alternative fabrication techniques, the metal layer has been restored, which resulted in a successful completion of the process flow. Various devices have been assembled upon a printed circuit board and characterised using a gain-phase analyser. The individual gains of the sensor have been recorded, as well as a differential read-out making use of the on-chip reference sensor. As anticipated, the frequency responses show typical high-pass filter behaviour. Moreover, when introducing isopropanol and ethanol to the sensor, additional gains up to 8.5 and 3.8 dB have been observed, respectively. However, the interpretation of these results do not completely correspond to the true value of their relative permittivities. Hence, detection of these fluids is possible, but the determination of their exact relative permittivities remains open for future work.



Measurement Setups for Angle Dependent MEMS Thermal Anemometers

T. Hackett, J. Schmitz, D. Alveringh, R. Sanders, T. v.d. Berg, L. Reints, J.Y. Choi

Measuring and calibrating small thermal flow sensors can be a slow process and require commercial wind tunnels or expensive apparatus. Two different solutions have been made to quickly and effectively characterize thermal flow sensors in a lab setting allowing for rapid process development. The first method uses a 3D printed wind tunnel that allows a fluid to pass parallel to a 2D in plane hot wire and calorimetric anemometer. The 3D print can be easily adjusted to fit over different PCBs and accommodate for wire bonds while being able to be tightened to prevent fluid leakage. The fluid speed is regulated by a mass flow controller and is ensured to be laminar. The 3D print can also be adjusted to change the angle of attack of the fluid as well as other geometric parameters in line with other thermal anemometer devices.

The second method is an improved set up from previous work and consists of a large diameter tube fitted with exchangeable fans and flow conditioner, a reference anemometer and temperature sensor. The device under test can be rotated to change the angle of attack and is measured using a lock in amplifier over a Wheatstone bride. The heater is kept at a constant temperature through a feedback loop and the change in power is recorded together with the lock in data on a PC. The fan speed can be changed from the PC through an Arduino as well as the temperature of the heater through a power source. This system allows for easy testing of the anemometers and ensures good laminar flow over the device under test. Different devices can be measured and the apparatus can be cheaply and easily made in an average MEMS laboratory requiring only a few extra materials. Both of these set ups are used to test MEMS thermal anemometers fabricated by bulk micromachining as well as CMOS anemometers.

Design and integration of ‘PureGaB’ on Germanium photodiodes in photonic integrated circuits

Vinny Hassan, Asma Attariabad, Lis Nanver and Jurriaan Schmitz

Total projected market share for Silicon photonics is $1.1B by 2027, with $478M from consumer health, $454M from datacenter applications, $115M from photonic computing & rest from rapid growth sectors such as Lidar (190% CAGR between 2020-2027). Critical components under active development are SiN for waveguides, LNOI for non-linear devices and Ge for detectors. This research work is dedicated to the design & integration of Ge photodiodes (PD) with ultra-high sensitivity & high bandwidth.

Inspiration for PureGaB (ultra-thin layers of B on Ga on 3.5 µm thick Ge) device is built on the successful development & implementation of PureB technology (< 10 nm pure B layer on Si). Driving force behind this innovation was to achieve low saturation current & defect density with sharper interfaces in an ultra-shallow junction. Formation of a complete layer of acceptor states at B/Si interface, leads to a high Gummel number & hole current density of the p+ region. This results in an extremely low electron injection from Si in forward bias and lower hole drift current in reverse bias regime, resulting in low saturation currents (on par with traditional deep junction diodes).

Research goal for the program is to reveal the mechanism behind the role interfaces (B/Ga & Ga/Ge) play, in determining the photodiode behavior. Application goal is the heterogenous integration of the PD in a photonic integrated circuit (PIC), with coupling loss < 0.1 dB & 30 GHz bandwidth. Three major challenges that needs to be addressed are: optimization of a fabrication process to pattern PureGaB/Ge PD, design test vehicles to decipher the interface charge properties & develop novel integration techniques for monolithic fabrication of PD in a PIC.

Design phase will revolve around process optimization of PureGaB/Ge PD, focusing on minimizing density of interface traps, inter-diffusion and defect density. The integration phase will concentrate on novel fabrication techniques of waveguide-PD coupling.

The overall project strategy will be using a two-pronged approach. The first pathway will be based on property-structure-deposition relationship, to optimize deposition/etching processes for PureGaB. The second pathway involves evaluating novel process ideas based on synchrotron x-ray characterization techniques such as ARPES, COBRA and EXAFS. Photo-generated current avenues, temporal evolution of interfaces during the photogeneration process, bonding configuration and interface-to-deposition relationships will be analyzed.

Investigating Palladium Reservoirs for Hydrogen-Enhanced Recovery of Hot-Carrier-Degradation

Max Krakers, Cora Salm, Jurriaan Schmitz

MOS transistor lifetime is largely dependent on the stability of parameters like Threshold Voltage (Vt) and Subthreshold Swing (SS). If these parameters shift, devices malfunction. One effect that changes these parameters over time is Hot Carrier Degradation (HCD) which places a hard limit on the lifetime of a device. One method to undo the damage caused by HCD is to perform thermal anneals. In the past, attempts have been made to link the Vt-shift recovery rate to the presence of H2 near the transistor. Here we investigate the effect of adding a H2 reservoir to our devices to investigate the possible link to H2 presence.

Our work focuses on using Palladium, which is known to absorb large amounts of H2, as the reservoir material. The Pd reservoir is capped with Al2O3 to prevent H2 out diffusion. The reservoir is placed on the backside of the chips to avoid shorts with other devices or metal traces, removing the need for precise alignment, and minimizing disruption of the normal fabrication process. Fig.1 shows the process flow used to fabricate the devices.

Our results in fig. 2 show that merely treating devices with a H2 anneal is not beneficial. However, the Al2O3 capped Pd reservoirs show a large increase in recovery of ~15% at shorter anneal times. This effect gets smaller over time as the untreated devices catch up. It is interesting to note that an uncapped reservoir, or just a capping layer, with a H2 anneal also has an effect. These small effects disappear rapidly when anneal times are increased. In conclusion, backside palladium works as a H2 reservoir and enables hydrogen-enhanced recovery of hot-carrier-degradation.

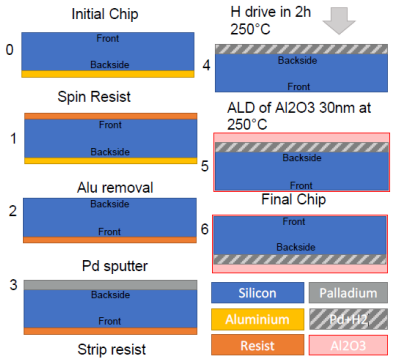


Fig.1 the fabrication process flow showing from 0 to 6 the steps taken to fabricate the DUTs

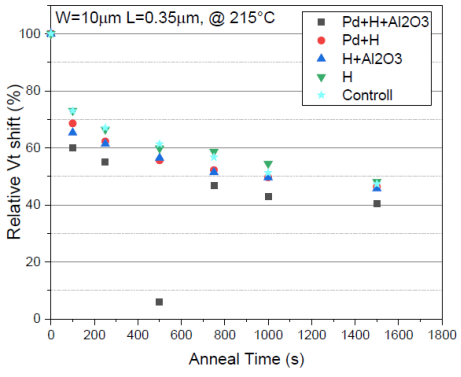


Fig.2 Normalised recovery behaviour of the DUTs, each stressed to ~330mV Vt shift. showing that reservoirs increase the rate of recovery.

An integrated optical method to readout µ-Coriolis mass flow sensors

Anneirudh Sundararajan, Remco J. Wiegerink, Remco G.P. Sanders, Qihui Yu1, Joost C. Lötters

This paper presents a novel readout for a µ-Coriolis mass flow sensor based on a differential optical reflective method, using chip based VCSEL (vertical-cavity surface-emitting laser) and two photodiodes. The new readout detects the ratio between the out-of-plane displacement and the rotation of the sensor tube by measuring the phase shift between the two photodiode signals. Such a setup offers a non-contact, low cost and robust sensing method. Measurements are presented for mass flow of DI-water (H2O) up to 10 gram/hour resulting in a phase shift of 8.7 degrees.

Micro-electromechanical systems (MEMS) based microfluidic devices, such as the µ-Coriolis mass flow sensor, have the potential to offer multiparameter sensing and miniaturization in the microfluidic domain for detecting several fluid properties. These devices have high sensitivity to low flow ranges, typically from 0.1 to 100 grams per hour. The capacitive readout is commonly used to detect the two vibration modes of µ-Coriolis mass flow sensors. However, this readout method is relatively fragile and sensitive to shocks and water hammering effects, which can lead to inaccurate measurements. An alternative robust, non-contact sensing method is needed to compensate for such effects during measurements. Integrated approaches using vertical-cavity surface-emitting lasers (VCSELs) and photodiodes (PDs) have shown promise in solving the miniaturization and compactness issue associated with optical readout of µ-Coriolis mass flow sensors. These optical components can be integrated directly on the chip to detect the linear and tilt motions. In this paper, we present a potential optical readout method based on a chip-based VCSEL and two PDs to detect the Coriolis movement of a µ-Coriolis mass flow sensor.

We will be using two photodiodes positioned on the left and right equidistantly from the VCSEL. The incident power received at the photodiode can be defined by integrating the derived reflected radiant intensity over the surface area of the detection region. The reflected light from the reflective surface passes perpendicular through the detection plane. Hence all the above calculations are carried out in sequence for the modified radiant intensity that is integrated over the detection region of PD-A and PD-B. Finally, the received optical powers at the photodiodes A and B which are crucial in designing a theoretical model for a compact optical readout system of a µ-Coriolis mass flow sensor.

The integrated setup was able to measure this change in flow with a resolution of 0.65 degree per 1 gram per hour for flow ranges upto 10 gram per hour at which the phase difference was around 8.7 degrees. The packaging proved to be low cost and robust. However only one type of fluid is tested for this work. A plan to carry out measurements with different type of fluid and gasses at both higher and lower flow rate is to be executed. The integration technique needs to be further optimized for better stability in alignment. A dedicated design for mass flow sensor with the reflective mirror and gratings can further solve in improving measurement sensitivity. Such approaches introduce integrated optical sensing to the existing multiparameter flow sensors.

Using Pure Boron Layers in Insulated Gate Bipolar Transistors

J. van Zoeren, T.T.H. Vu, L.K. Nanver, R.J.E. Hueting

In the last couple of years, the demand for power electronics has drastically increased. Many emerging technologies require these power electronics to be more energy efficient, lower in cost and smaller in size. Important examples of these emerging technologies are the electrification of our transport and the transition to renewable energy sources.

A promising material for applications in power semiconductor devices is an ultra-narrow layer of boron (PureB). About one decade ago, it was found that it advantageous electrical properties. Until then, most of the research on boron was focused on the p-type dopant properties. The exact working mechanism of this PureB layer has yet to be confirmed, but there is strong evidence that this material creates a fixed negative charge at the semiconductor interface. As a result, a dense hole accumulation layer is formed which dramatically suppresses the electron injection. These PureB layers are electrically and chemically very robust, and can be deposited within a broad temperature range from 700°C down to 50°C. Furthermore, the PureB layer has also be shown to be a diffusion barrier for different metals such as aluminium.

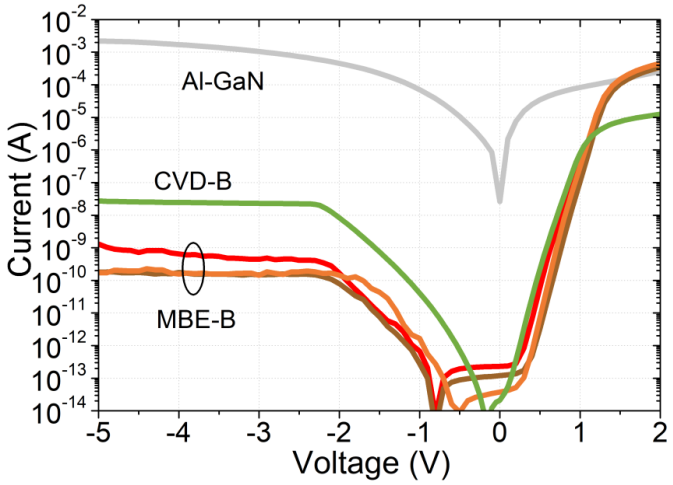
Nonetheless, the application of PureB layers in power semiconductor devices has not been extensively studied. In the B-power project, my main focus is on Insulated Gate Bipolar Transistor (IGBT) devices. IGBTs are the main power devices in the range from a few hundred volts up to several kilovolts, with applications in renewable energy, transportation, appliances and industry. The adoption of PureB in an IGBT collector could provide a higher emitter efficiency and a lower resistance, hence lower power losses, whilst also having processing advantages over the implantation process.

A clear trend in the IGBT collector is that with increasing collector doping concentration (or Gummel number), more charge plasma is formed under high injection conditions. Having a higher charge plasma decreases the on-resistance of the IGBT, but decreases the switching speed. This is one of the most important trade-offs in IGBTs [8], but the underlying principle has not been described well in literature. Therefore, it is important to study this behaviour to further understand the application of PureB in such a collector. Lastly, devices will also be processed in the MESA+ cleanroom, after which thorough characterisation and simulations will be performed to study the PureB behaviour and build upon the existing PureB TCAD model.

Batch furnace CVD of pure boron layers on Si and GaN substrates for low-leakage-current diode fabrication

Thi Thanh Huong Vu, Kevin M. Batenburg, Antonius A.I. Aarnink, Tihomir Knežević, Xingyu Liu, Lis K. Nanver

Boron deposition on both n-Si and n-GaN in the temperature range 250 - 500 °C, has been shown to form diodes with low saturation currents, i.e., electron injection from the n-substrate into the B-layer was efficiently suppressed. Moreover, down to 3-nm-thick B-layers on Si were shown to form a material barrier to Al, opening the possibility of fabricating Au-free gates for gallium-nitride high-electron-mobility transistors (GaN HEMTs). Several different chemical- and physical-vapor deposition (CVD/PVD) methods for depositing B have been studied for fabricating p+n-like Si diodes, called PureB diodes, all with comparable results. In this paper, the deposition of B-layers from diborane in a CVD batch furnace system is evaluated, particularly for use as a barrier material to enable Al-contacting of GaN diodes. These Al-B diodes could provide an option for fabricating low-leakage diodes that are compatible with complementary metal-oxide-semiconductor (CMOS) processing at industrially attractive high throughput. The bulk B has high resistivity, which, combined with the fact that non-uniformities in the nm range are typical due to gas depletion along the furnace tube, gives uncontrollable, often high diode series resistance. A simulation study shows that Al-B could, nevertheless, be used as a gate stack in HEMTs for low-frequency power applications.



Diode *I-V* characteristics for GaN diodes; without B-layer, with CVD-B grown at 450 ?C, and with MBE-B grown at substrate temperatures of 250 ?C, 350 ?C, and 400 ?C.

Film growth and carbon-tunability of ALD processed alumina (Al2O3)

Weihua Wu, Jiamin Wang, Antonius A.I. Aarnink, Jurriaan Schmitz, and Alexey Y. Kovalgin

ALD film growth for aluminium oxide (Al2O3) has been widely studied starting from trimethylaluminum (TMA) and water. The formation of metal oxide (MO) bond is dominated by the alternative legend exchange between methyl (CH3) groups and hydrogen (H) from TMA and water, respectively. It's usually an efficient process for the removal of the added carbon from CH3 groups in this system as its content would be less than 1 at.% especially at temperature below 350 oC. In those cases, carbon would generally be treated as unwanted impurity and show less pronounced effects on film properties. While the incorporation of carbon to some amount may also show added benefits to the film properties as it can form possible chemical bond with the cation or anion in ALD process, which leads to partly carbides or oxy-carbides. Hence, this work aims to provide feasible ALD solution to tune the carbon concentration inside Al2O3 and deeper understanding on its impact to the film properties (such as surface morphology, optical bandgap, etc).

To efficiently tune carbon inside Al2O3, two different strategies are considered in this work. First strategy is to activate the carbon supply in purely thermal ALD by applying deposition temperature higher than the thermal decomposition onset of TMA (~340 oC). Second strategy is to further inhibit the formation of MO bond by decreasing the supply of oxidants and providing a reductive environment by adding atomic hydrogen to the reactor. Here we use TMA and hydrogen plasma (H-plasma) to incorporate carbon inside the film with the hope of promoting possible (oxy)carbide bonds formation.

With the temperature up to 400 oC, following the first strategy, we noticed that a thickness of approx. 1.6 nm was needed to reach the closure point of the film on H-terminated Si substrate. The carbon concentration was below the detection limit of XPS (0.1 at%) as checked by in-depth profiling, which indicated the efficiency of carbon removal via this process. In this work, film growth feasibility and tunability of carbon share in carbon-doped alumina (Al2O3:C) will be further revealed by following the second strategy, in which we intend to vary deposition temperature, plasma composition, and plasma pulse time. This work and the knowledge gained will contribute to studying ALD of other metal oxides in view of considering carbon incorporation in such materials.