Research Statement

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Over the years I've been involved in computer engineering topics varying from *computer aided design* to *computer architecture*, *logic design*, and *implementation*.

In the first decade I worked in research & development (co-)initiating, implementing, and documenting innovative ideas and techniques in *software* development. Have been involved in the research of new algorithms and techniques for *computer aided design* of Integrated Circuits (ICs). In particular I've worked in: *design rule checking*, *layout generation*, *logic* and *mixed simulation*, *test generation* and *testability analysis*, and *image processing* for visual inspection of IC masks.

After relocating to the Netherlands in October 1993 I started my real researcher career as a PhD student at Delft University of Technology and I have been involved in research investigations in logic design and implementation of *computer arithmetic* operations with *linear threshold logic*, *multimedia* and *vector architectures* and processors, interconnection networks and routing algorithms for *parallel processors*. I have also worked in the engineering of *superscalar machines* on open questions related to the design complexity of the parallel issue logic.

1 Current Research

My current research is focussed on the *design and implementation of dependable/reliable systems out of unpredictable/unreliable components*. In view of that I am addressing various topics from *nano-electronics* and nano-device specific *design methodologies* and *fault tolerant computational paradigms*, *parallel processing* and *programming models*, *embedded systems*, *reconfigurable computing*, *computer arithmetic*, *low power* hardware, *power management*, and *multimedia and vector* architectures and processors. More in particular I'm focussing on the followings:

- Investigation on architectural and runtime support for non intrusive observation and adaptation mechanisms for dependable computation able to enable various performance-power-reliability policies and tradeoffs (COBRA).
- Investigations on reliability aware computation platforms and reliability (life time) prediction models (RELY).
- Investigations on 3D system architectures for Multimedia and Mobile applications (3DIM3).
- Investigations on scalable, composable, predictable, and energy-aware multi-core platforms for embedded applications (SCALOPES).

- Investigation on RNS arithmetic units.
- Investigations on the impact of 3D integration on computation platforms with emphasis on architecture and reliability aspects.
- Investigations on multi/many core platforms with emphasis on architectural and run-time mechanisms for variability and reliability aware resource management.
- Investigations on the utilization of Nano-Electro-Mechanical (NEM) structures, e.g., suspended gate FETs, in sleep mode circuits and *power management* with an emphasis on *wireless sensor nodes* and networks.
- Investigations on *application mapping* and *programming models* for *muti-core platforms* with emphasis on the MOVIDIA architecture.
- Investigations on *design methodologies* and *computation platforms* for *nanoelectronics*. Theoretical contributions related to design methodologies for fabrication parameters variability (the Casta DIVA paradigm), and to reliable computation with unpredictable devices (the CONAN platform).
- Investigations on novel *computation paradigms* for *nano-devices*. Theoretical and practical improvements related to the computation of arithmetic functions, e.g., addition, counting, multi-operand additions and multiplication, via direct *charge manipulation*.
- Investigations on the realization of Boolean function with *Single Electron Technology* (SET) based gates. Theoretical and practical improvements related to the SET based realization of logic gates, memory elements, analog-to-digital and digital-to-analog conversions, addition, and multiplication.
- Investigations on Multiprocessor platforms and Networks on Chip (NoC). Theoretical and practical improvements related to *cache management* in memory hierarchies for achieving *system compositionality*.
- Investigations on *low power architecture* and circuits for *mobile computer graphics* applications. Theoretical and practical improvements related to the hardware implementation of the rasterization stage of the *3D graphics* pipeline and to design space exploration methods appropriated for 3D graphics hardware design.
- Investigations on the *reconfigurable computing* paradigm. Theoretical and practical improvements related to processors architecture that embed an *FPGA* based reconfigurable core.
- Investigations on *multimedia/embedded processors*. Theoretical and practical improvements related to the MPEG related performance of FPGA enhanced *TriMedia* processors.

- Investigations on the implementation of *high-speed*, *low-power* with *high fan-in and weights* capabilities *linear threshold gates*. Theoretical and practical improvements related to the standard CMOS implemented low-power and high fan-in linear threshold gates.
- Investigations on *hybrid Boolean and Threshold logic* schemes for arithmetic operations. Theoretical and practical improvements related to the implementation of counters, adders, and multipliers.

2 Future Plans

The main goal for the future is to pursue innovation in *computer technology* in general with emphasis on hardware related topics.

As general research policy I like to probe the future via *speculative* research projects while still remaining well anchored in nowadays technological reality. In this line of reasoning I consider a good balance between speculative research aimed to stretch the technological limits of computer technology, thereby considering a long term horizon, and *short term (applied)* research of premium importance. Additionally, I consider the collaboration with industry as an important objective for applied research as well as for more speculative projects.

Interdisciplinary Cross-fertilization

I believe that a significant part of tomorrow's innovations will be the result of interdisciplinary projects via cross-fertilization and domain synergy. My past experience strongly support this (due to my mixed Computer Science (CS) and Electrical Engineering (EE) background I mainly carried research at boundaries between this two domains) and I plan to stick with this strategy.

Furthermore, I intend to extend the multidisciplinary dimension by considering research projects where more than the EE and CS fields are considered, e.g., bio-inspired and molecular computing. I see this extension as a natural consequence of recent developments in nano-materials. These new nano-technologies offer numerous alternative ways to do computation thus the EE-CS community should be prepared for the moment when they will become mature thus potentially utilizable in building information processing systems.

Novel Devices, Novel Paradigms

Currently, there is a wide gap between research on nanoscale devices and research on their utilization in computer technology. Essentially these new nanodevices appear to exhibit behaviors that are substantially different than that of the well established MOS devices and this in my opinion calls for novel computation paradigms and design methodologies.

In my opinion the tomorrow's replacement of the MOS transistor will not just be an MOS alike device build with a different technology. I certainly understand the reasons why the industry might be reluctant to such a major paradigm change (evolution is always preferable to revolution) but if we are to fully utilize the potential of these emerging devices we should adapt the paradigms to their specifics.

It is by no means my intention to suggest that traditional CMOS based electrical and computer engineering will cease to exist in the near future but I think one has to keep pace with the new emerging technologies as eventually they will become dominant.

Unpredictability, Variability, Reliability, and Fault/Defect Tolerance

Another problem inherent to very small (nano scale) devices that will certainly change the way we design and programme computer systems is induced by device parameter variations and by their expected low reliability. Together with some other sources of variance, e.g., temperature and power supply variations, these parameter variation cause significant fluctuations in the time required by a part of a circuit to perform its computational task. Up till now, delay variations have been mainly dealt with by using over-design, i.e., sufficient large margins are used to ensure that each part of the chip has enough time to finish its work. As the impact of delay variations increases with downscaling, for near future technologies this will lead to excessive margins, resulting in large performance losses (a generation of fabrication technology improvement can be lost).

Therefore, I think that research related to introspective generic architectures and associated design methodologies that enable circuit and system designers to seamlessly incorporate design for variability and design for reliability in their designs is of premium importance for deep submicron CMOS fabrication technologies as well as for other alternative nano-technologies.

Parallelism, Reconfiguration, and Programming Models

Last but not least, another important issue, also boosted by fabrication technology developments, which may change the way computation will be done in the near future is the possibility to construct highly parallel, fault tolerant, and reconfigurable structures which may or may not follow "traditional" organizations.

Even though many problems have still to be solved in this domain (while many proposals exist the architecture of such highly parallel systems is still an open research issue) I expect that major changes have to be operated in the way one programs and maps applications on such platforms. To deal with the increased complexity of the modern applications and to be able to effectively exploit the huge amount of available resources, while keeping the pace with a very dynamic market, one needs the appropriate tools and also a change in perception and mentality.

Having the previously stated thoughts as part of my research credo my future research will continue to focus on the design and implementation of dependable/reliable systems out of unpredictable/unreliable components. As I strongly believe that this goal can only be reached if the problem is addressed at various levels, thus the solution will come from a synergetic approach (domains and abstraction levels), I foreseen that the following fields will (continue to) constitute the main focus of my future research:

- Nano-electronic fault tolerant computation platforms.
- Technology aware design methodologies that can handle parameter variations.
- Self-adapting systems that can address (predict and manage) issues like device/system reliability and thermal phenomena.
- Towards ”zero energy” computing architectures and circuits.
- Uncertainty tolerant and noise driven computing.
- Many/multi-core architectures and programming paradigms and system design methodologies for highly parallel computation platforms.
- Bio-inspired evolvable computing paradigms and circuits.
- Polymorphic hardware and custom computing machines.
- Multidimensional (hardware-reconfigurable-software) co-design.
- Energy aware computation (low-power circuits and systems, power & temperature management).
- Embedded systems and processors.
- Computer arithmetic.
- Programming models for unconventional computing paradigms.