Programming FPGAs with MaxJ

Two-day course for researchers, PhD and MSc students

September 23-24, 2019

What is an FPGA? Field Programmable Gate Arrays (FPGAs) are reconfigurable chips, which facilitate direct implementation of algorithms (or their data intensive parts) as hardware circuits. This enables the development of application specific hardware accelerators, delivering high throughput, low energy and constant latency to solution and very fine grain control over all basic arithmetic operations, their sizes and properties. FPGA based systems enable highly customised, application specific dataformats for each individual fixed and floating point variable but is not limited to the above two types. As a result, FPGA accelerators have seen a rapid adoption by both Industry and Academia especially in the context of high performance computing. The efficient design for FPGAs based systems, however, combines three distinct knowledge areas: i) the application specific system architecture to maximally utilise all available compute and interconnect capabilities; ii) dedicated programming tools and languages; and iii) FPGA specific design and programming methodologies.

What is MaxJ? MaxJ is a Java based programming language used to leverage the dataflow abstraction for high performance computing. The programmer describes a custom dataflow graph which is translated to a hardware circuit. The MaxJ toolchain provides easy to use framework aimed at domain experts and not hardware engineers.

Goals and prerequisites To guide you in this development niche, the TU Delft Institute for Computational Science and Engineering (DCSE) offers a 2-day course. We will explain the basic principles and some advanced topics on FPGA programming with MaxJ. You will apply these notions in our labroom with hands-on examples. After this course you will be able to successfully benefit from dataflow computing to your own work.
As prerequisite, a rudimentary understanding of programming languages like C++ or Java is ideal. Some interest in computer architecture, computer arithmetic and numeric analysis is of additional advantage.

Instructors and schedule Prof Georgi Gaydadjiev (GG), Mr Nils Voss (NV) from Maxeler IoT-Labs BV and Dr Christos Strydis (CS) of the Neuroscience department of the Erasmus Medical Centre will teach this course.

	Basic principles (day 1)		Advanced topics (day 2)	
09:15–09:30	Arrival: refreshments		Arrival: refreshments	
09:30–10:30	Introduction to Dataflow Computing	GG	Use Case: Brain Simulation using Dataflow	CS
10:45–11:30	Using Maxeler Dataflow Engines	GG	Loops and Arithmetic in Space	GG
11:45–12:30	Programming Dataflow Engines	GG	Modeling and Optimising Dataflow Engines	NV
12:45–13:30	Lunch		Lunch	
13:30–17:00	MaxJ Programming Exercises (Part 1)	NV	MaxJ Programming Exercises (Part 2)	NV

Location Delft University of Technology, Faculty of Mathematics & Computer Science, Van Mourik Broekmanweg 6, 2628 XE Delft. The classes are given in Building 28, 'Penguin' Laboratory Room (E0.380).

Costs and registration The course is free for DCSE members. TU Delft staff and students pay € 50/100 for attending one/two-day(s) respectively. The fee for other participants is € 200/350. Lunch, refreshments, lecture materials are included.
Please sign up at https://www.aanmelder.nl/fpgacourse. The maximum number of participants is 20.

Additional information Splash page: https://www.tudelft.nl/cse/education/courses/fpga-course/.
Contact: G.N.Gaydadjiev@tudelft.nl for questions related to the content or
dcse@tudelft.nl for administrative and logistics matters.
Bring your own laptop with pre-installed VirtualBox. We advise you to attend both days.

DCSE Delft University of Technology